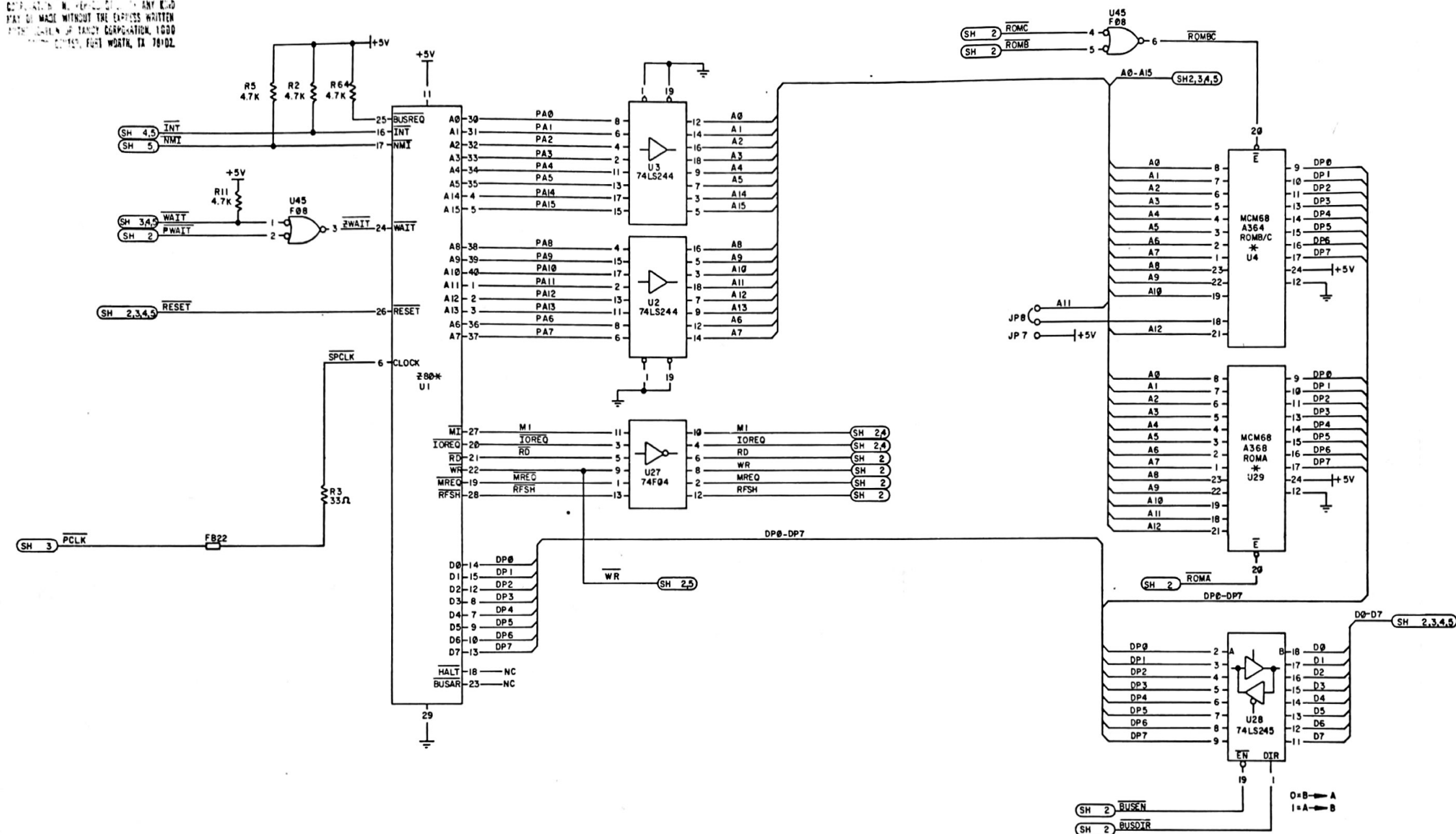


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ZONE	LTR	REVISION	DESCRIPTION	DATE	APPROVED
		1	RELEASED FOR PRODUCTION	4-10-84	



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PAGE 1-	CPU, ROM, & MAIN BUFFERS
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PAGE 4-	KEYBOARD, LINE PRINTER, I/O BUS, & CASSETTE INTERFACES
PAGE 5-	DISK & RS232 INTERFACES

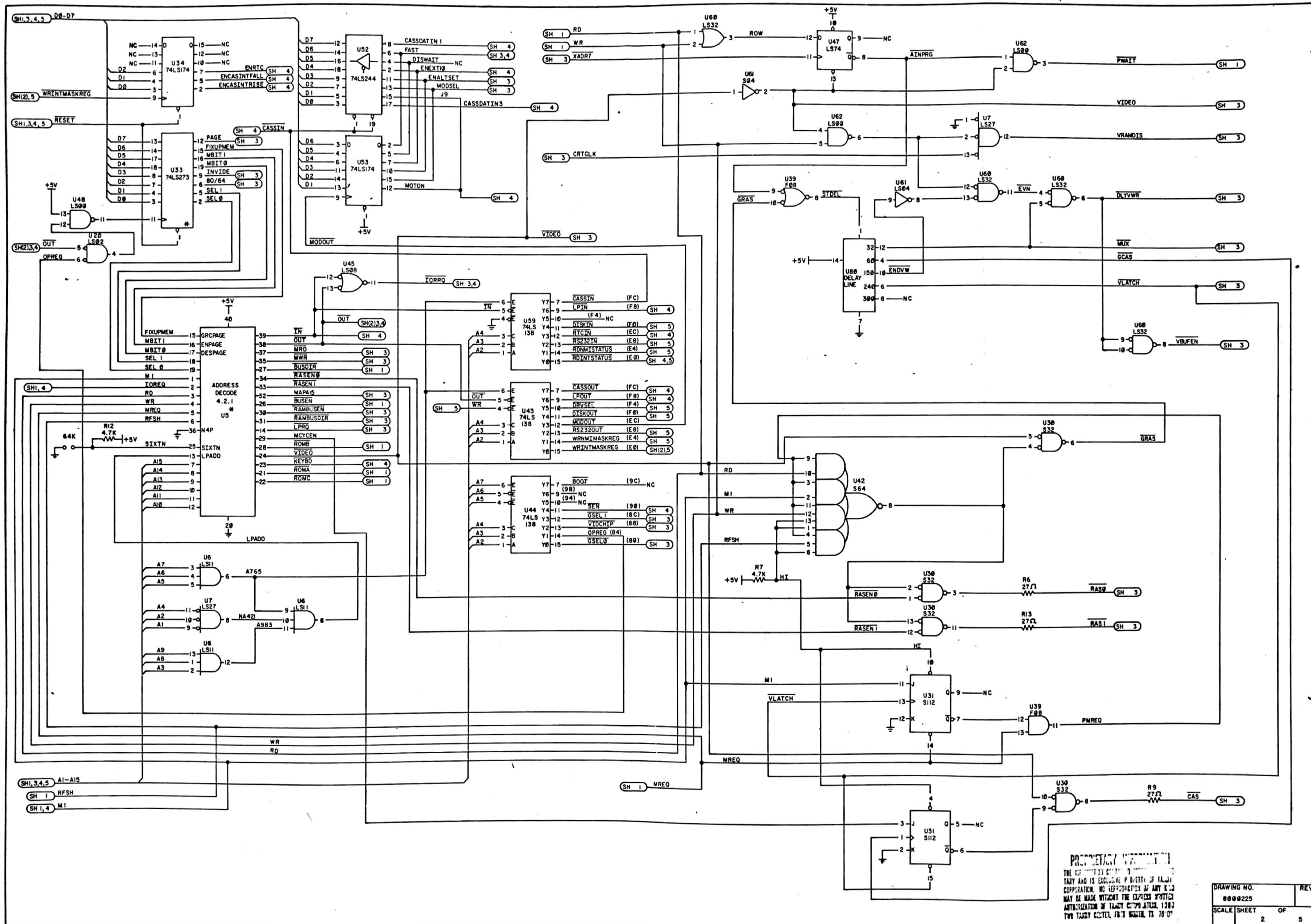
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REF. DRILL PLAN 1700277 RE2A

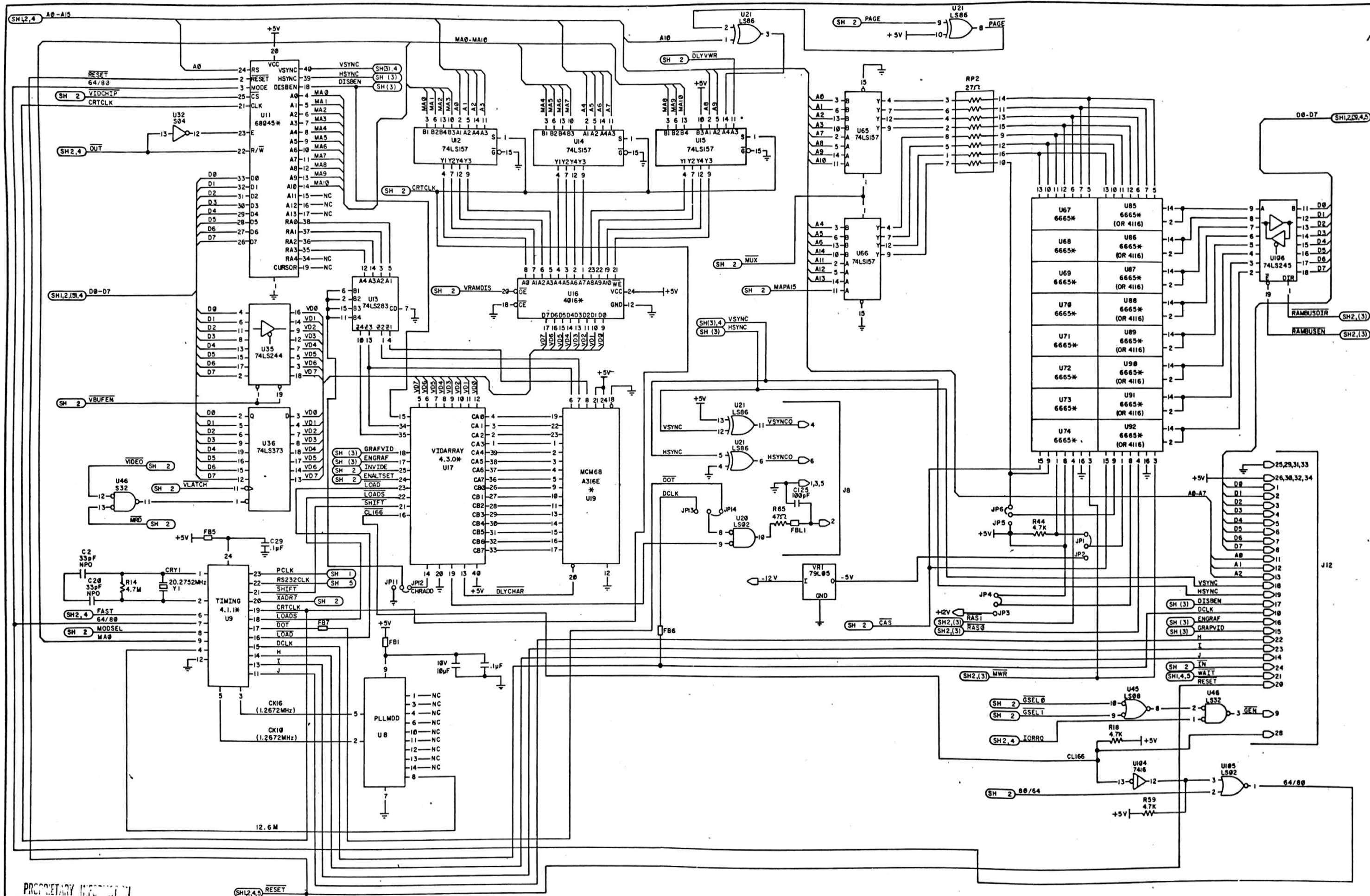
DATE	BY	DATE	BY	TITLE
2/22/83	STEPHEN D. MATFIELD	2/22/83		SCHEMATIC—
4/1/83		4/1/83		GATE ARRAY
4/1/83		4/1/83		MODEL 4
4/1/83		4/1/83		26-1069A

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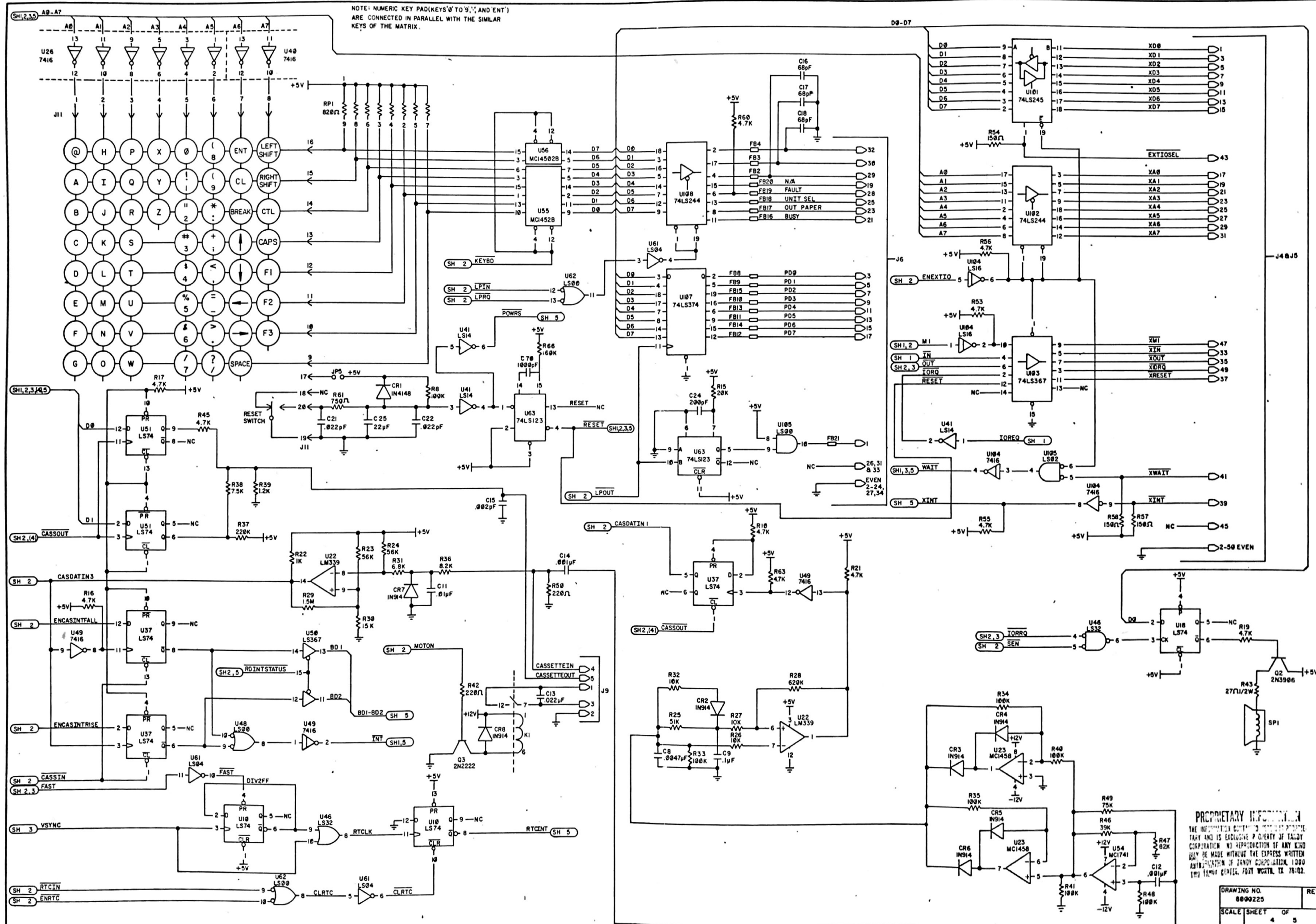
DWG NO	8000225	SHEET	1	OF	5
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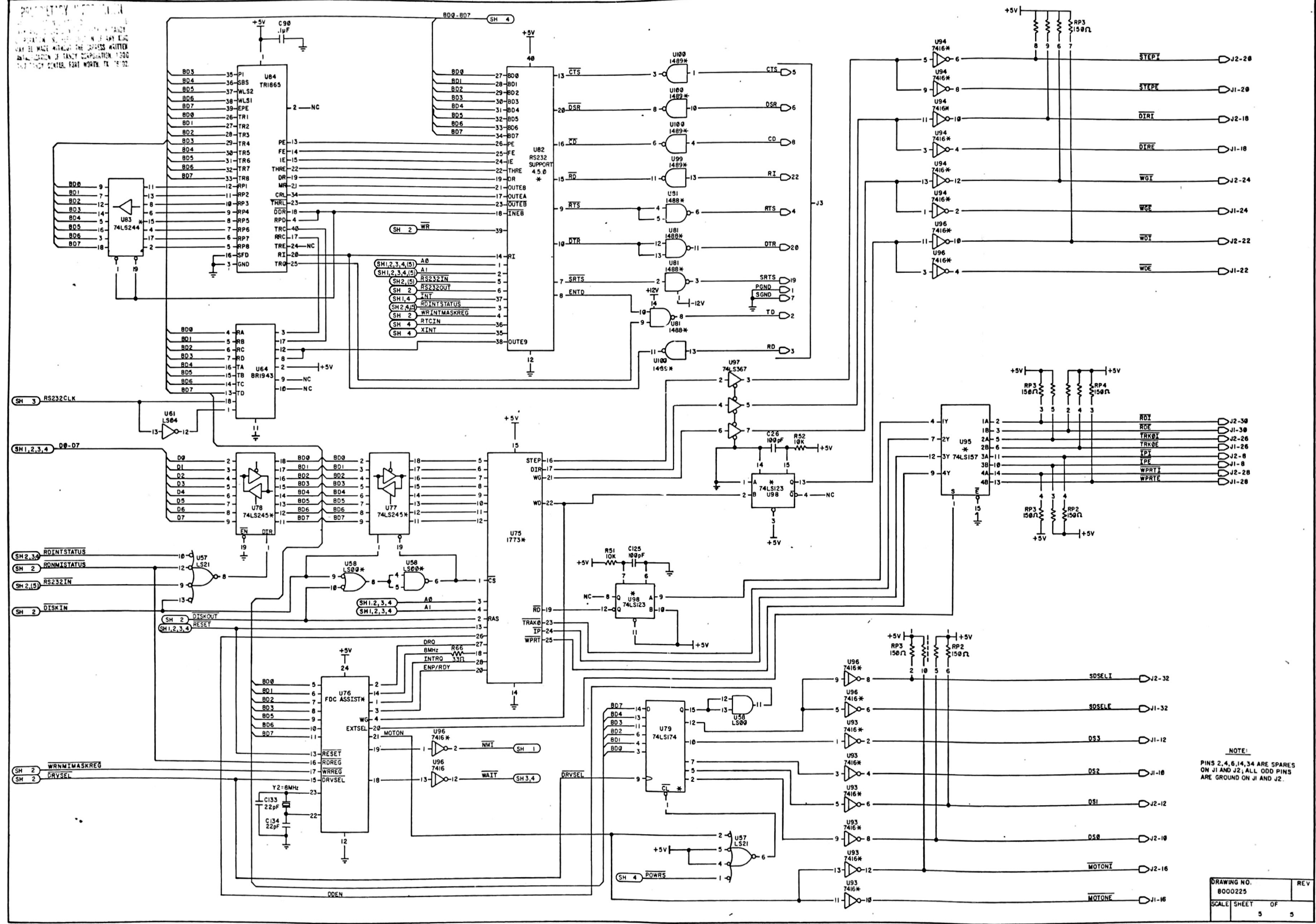
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NOTE:
 PINS 2, 4, 6, 14, 34 ARE SPARES
 ON J1 AND J2; ALL ODD PINS
 ARE GROUND ON J1 AND J2.