Radio Shack®

TECHNICAL INFORMATION SERIES

TRS-80®

MODEL II GLOSSARY

0220 TECHNICAL SUPPORT SERVICES

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Introduction

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This manual is divided into five sections:

CPU Board.....Section 1

FDC (Early) Board.....Section 2

FDC (Late) Board.....Section 3

VDG Board.....Section 4

Memory Board.....Section 5

Each section contains a glossary on most of the mnemonics listed on the respective schematics contained in the Model II Technical Reference Manual.

Most of the sections also contain Port Allocation Tables, Test Point Definitions, and Standard Jumper Configurations.

This Glossary is not intended as an indepenant tutorial, but is rather a supplementary service aid to the contents of the Model II Technical Reference Manual.

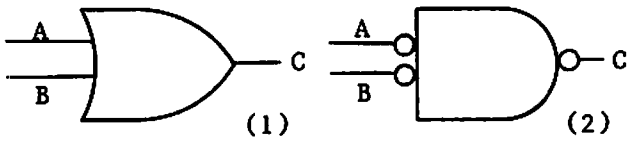
Model II Technical Bulletins referenced in several sections of the Model II Glossary© are contained in the newly issued TECHNICAL BULLETINS, Volume 1.

Notes on Conventions used in the Model II Glossary©

In the schematics for the Model II, it is a convention to indicate in the name of "single action" control signals the logic level which is required to initiate other activity. Thus, for example, MREQ* and RD* from the Z8Ø indicates that logic lows will initate the sequence of activities that will result in data from memory being placed on the data bus, while MREQ and RD would indicate initiation of activity at logic highs. In this Glossary, the word "asserted" will be used to indicate such a logic level (i.e, logic low for MREQ*), while the word "negated" will be used to indicate the logic level which does not initiate activity, or which terminates activity (i.e., logic high for MREQ*).

This convention is not used for "dual action" control signals, since both levels will produce a desired result. For example, a logic high DIR will cause a drive head to move inward toward Track 76, while a logic low DIR will cause the head to move outward toward Track Ø.

In the schematics for the Model II Boards, many logic gate symbols are shown with inversion bubbles on the input side of the gate. The logic symbols for such gates shown in the chip specification sheets, however, are not the same. For example, a function of a Quad 2-Input OR Gate, such as the 74LS32, would normally be drawn as in Diagram 1 below, but on the schematics it might be drawn as a NAND gate with two bubbles on the input side as in Diagram 2, below. Both symbols yield the same truth table shown below, and are thus functionally equivalent. Note that the negative logic equivalent to the positive logic OR gate is the AND gate: thus Diagram 2 is not the negative logic equivalent for Diagram 1.



A	B	C
Ø	Ø	Ø
1	Ø	1
Ø	1	1
1	1	1

The purpose of using a functionally equivalent-type of symbol is to emphasize the logic inputs necessary to create the logic output that will represent the asserted level of a signal from the gate. In the example of Diagram 2, a logic low represents the asserted level from the NAND gate: both inputs must be low to obtain this asserted output level.

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Section One

Model II CPU Board

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Contents

The listings in this glossary are divided into 3 sections, respective to the three sheets of the CPU schematic.

When a signal from one sheet is referenced to another, a pointer, "/#", will be used to indicate the sheet: i.e. From Pin 1 of U14/2 To Pin 24 of U12/1.

The CPU schematics reflect the circuitry of the REV B Board. The latest CPU Board is REV D.

Index for CPU Board Signals

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Glossary - Sheet 3

Only the mnemonics originating from Sheet 3 of the CPU schematic will be covered under this heading.

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F9* From Pin 11 of the Port Address Decoder U36. To Pin 2 of U37, and Pin 13 of U3. When asserted, this signal indicates that the CPU is in the process of selecting or deselecting the Boot ROM. See "SHADOW*".

F8* From Pin 1Ø of the Port Address Decoder U36. To Pin 4 of U37. Also routed to Pin 1 of U3/1 as signal "CEDMA*". When asserted, this signal indicates that the CPU is in the process of transfering control or command data to or from the DMA.

F4*-F7* From Pins 5, 6, 7, and 9 of Port Address Decoder U36. To Pin 5 of U37. Also routed to Pin 35 of U18/2 as signal "CESIO*". This signal indicates that the CPU is in the process of writing commands or data to or from the SIO. The SIO will transmit data to the CPU when this signal is asserted during a Read cycle.

FØ*-F3* From Pins 1, 2, 3, and 4 of the Port Address Decoder, U36. To Pin 1 of U37. Also routed to Pin 16 of U19/2 as signal "CECTC*". When asserted during a Port Write, this signal indicates that the CTC is in the process of accepting control words, interrupt vectors, or time constant data words from the Bus. During a Port Read, this signal indicates that the CTC is transmitting data from one of its Down-Counters to the CPU.

I/O ADD* From Pin 12 of U17. To Pin 1 of U16. This signal detects when any of the on-board Ports is being addressed.

IN* — From Pin 6 of U5. When asserted, this signal indicates that the CPU is in the process of doing a Port Read. To Pin 9 of U14 where it is ORed with "OUT*" (see same) to become signal "IN*+OUT*" (see same). "IN*" is also used in the Bus Steering Logic at Pin 13 of U22.

OUT* — From Pin 3 of U5. When asserted, this signal indicates that the CPU is in the process of doing a Port Write. To Pin 1Ø of U14 where it is ORed with "IN*" (see same) to become signal "IN*+OUT*" (see same). Also used at Pin 12 of U3 where it is ANDed with "F9*" to become signal "SHADOW*" (see same).

LOW 4K* — From Pin 11 of U5. When asserted, this signal indicates that the System Address space between 1ØØØH and FFFFH is not being accessed. To Pin 1Ø of U5 where it is ANDed with signal "ROM*/RAM" (see same) to enable the ROM gates.

READ* (TP 4) — From Pin 8 of U3. This signal will be asserted during a Memory Read cycle. To Pin 13 of the Read ROM Gate, U16. Also routed to Pin 2Ø of U11/1, where it is used to enable the ROM Data output lines.

RDROM* — From Pin 11 of U16. A conditional signal to Pin 12 of the Select Gate U14. Asserted during a Memory Read cycle when the CPU is in the process of accessing the System Address space between ØØØØH and ØFFFH.

ROMØCE* (TP 3) — From Pin 6 of U16. Chip Enable signal for the Boot ROM. To Pin 18 of the Boot ROM U11. This signal will be asserted when "ROM*/RAM" is a logic low, and when the CPU is in the process of doing a Memory Read in the Address space between ØØØØH and Ø7FFH, or the first 2K of the System Memory.

ROM1CE* — From Pin 8 of U16. Chip Enable signal for a second 2K of ROM. This signal would be asserted in the Address space between Ø8ØØH and ØFFFH. Not currently used in the Model II.

SELECT* (TP 15)

From Pin 11 of U14. This signal will be asserted when the CPU is in the process of doing an on-board Port Select, or ROM Read. To Pin 1 of U39/1 through which it is presented to Pin 43 of the System Bus. Signal "SELECT*" at Pin 43 of the System Bus is not used by any external device.

Also to Pin 9 of the Bus Steering Gate U22, where it is used (TP 17) to disable the Receivers of the CPU Board Data Buffers U31 and U32 to prevent data from the System Bus from being received while the CPU is in the process of doing an on-board Port Select or ROM Read.

INTAK* (TP 13)

Pin 11 of U21. This signal will be asserted when the CPU is in the process of acknowledging either an on-board or an external Interrupt Request.

To Pin 3 of U13 (see note below). Also to Pin 2 of U21 where it will place Pin 1Ø of U22 at a logic low to disable the Receivers of the System Data Buffers when an on-board Interrupt Request is being serviced.

Note: Signal "INTAK*" is ANDed with signal "EIOUT" if the INTRQL Mod on the CPU Board is applied for BISYNC, HD, etc: refer to Technical Bulletins II:17 and II:26 for details. This circuitry is etched onto REV D and later Boards.

When an external device is generating the Interrupt Request, Pin 1Ø of U22 will remain at a logic high. At this same time, Pins 9 and 11 of U22 will also be at a logic high, and the Receivers of the Data Buffers will be enabled.

DMA EXT*

From Pin 6 of U3. To Pin 9 of U17/1 to disable the Drivers of Buffers U33, U34, and U35. Also to Pin 1Ø of U4 to disable the Drivers of Buffers U31 and U32. Not currently used in the Model II.

This signal would be asserted during an external device DMA operation, signified by signals "BUSRQ*" and "BAO*" (see same) being asserted at the same time. Were an external device DMA operation in progress, the Data, Address, and Control Drivers noted above would be disabled.

SHADOW*	From Pin 11 of U3. This signal will be asserted during a Port Write to "F9*". It is applied to Pin 11 of U13/2 as a clock to select or de-select the Boot ROM. The selection will depend on the logic status of Data bit Ø. See signal "ROM/RAM*".
IEOUT	To Pin 14 of the Model II System Bus. From Pin 24 of U24/1, where it is labeled "EIOUT". See Glossary, Sheet 2 and Sections 2 & 3, Early/Late FDC Boards.
EIIN	From Pin 13 of the Model II System Bus. There is no indication that this signal is used on the CPU Board.
BAKIN*	From Pin 15 of the Model II System Bus. There is no indication that this signal is used on the CPU Board.
BUSRQ*	From Pin 17 of the Model II System Bus. See Glossary, Sheet 1.
DISRO*	From Pin 4Ø of the Model II System Bus. There is no indication that this signal is used on the CPU Board. See Section 5, Memory Board.
KBIRQ*	From Pin 42 of the Model II System Bus, from the VDG Board. To Pin 2Ø of U19/2. See Glossary, Sheet 2.
WAIT* (BUS)	From Pin 48 of the Model II System Bus. To Pin 1 of U14/2 and to Pin 12 of U4/2. See Glossary, Sheet 2.
RTC	From Pin 47 of the Model II System Bus, from the VDG Board. It is mislabeled as going to Sheet 2: there is no indication that this signal is used on the CPU Board.

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Glossary - Sheet 2

Only the mnemonics originating from Sheet 2 of the CPU schematic will be covered under this heading.

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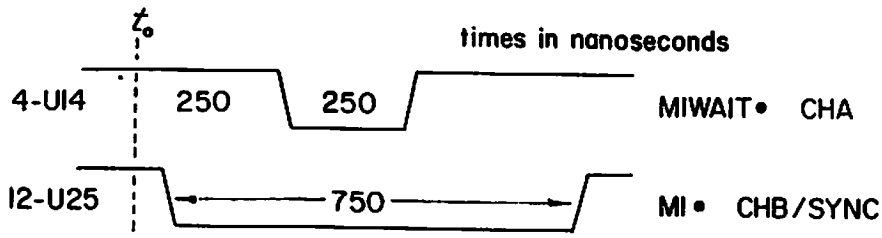
WAIT* (TP 12) — From Pin 3 of U14. To Pin 24 of the CPU U12. This signal is the logical result of an on-board Wait, or a Wait generated by an external device.

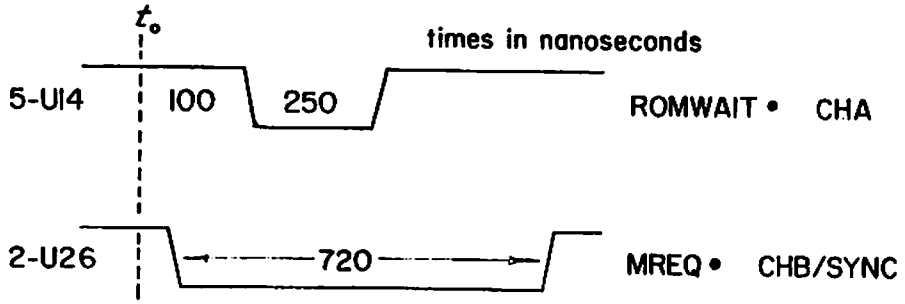
The Wait from an external device enters the CPU card at Pin 48 of the Model II System Bus. For the on-board Wait, see signal "OBWAIT*".

OBWAIT* — From Pin 6 of U14. The ORed result of an on-board Wait generated during either an Op-Code Fetch cycle from RAM or during any ROM Read.

The measured timing diagrams below illustrate how a Wait is generated during an Op-Code Fetch cycle from RAM. This Wait is required to permit extension of the pre-charge period prior to memory refresh occuring in the M1 cycle. See Section 5, Memory Board.



The measured timing diagrams on the next page illustrate how the Wait is generated during a ROM Read. This Wait is required to extend the period that signal "READ* at Pin 8 of U3/3 is asserted to permit assertion of valid data from the 3ØØ nanosecond ROM.



ROM/RAM* From Pin 9 of U13. To Pin 5 of ROM Wait Gate U22. Also to Pin 1Ø of RAM Wait Gate U21.

A Power-On, or Manual Reset at Pin 1Ø of U13 will set this signal to a logic high, indicating that the Boot ROM is selected. This condition will enable the ROM Wait Gate and allow the ROM Wait Generation Logic to output a Wait with every ROM Read. See "OBWAIT*" for the timing diagrams.

The Boot ROM will electrically switch out of the system when "SHADOW*" (see same) is initiated with Data bit Ø set at a logic low. This condition will now block the ROM Wait Gate. The Wait Generation Logic will now output Waits with every Op-Code Fetch. See "OBWAIT*" for the timing diagrams.

ROM*/RAM (TP 18) From Pin 8 of U13. This signal is the inverse of signal "ROM/RAM*" (see same).

To Pin 9 of U5/3. When the Boot ROM is selected, this signal will allow signal "LOW 4K*" (see same) to enable the ROM gates, which are three parts of U16/3.

Switching the Boot ROM out of the System will block signal "LOW 4K*". Thus, the first 4K of Address space can now be used to access the System RAMs.

RESET* (TP 11) From Pin 4 of U29. This is the System Reset signal. It is initiated during a Power-On, or Manual Reset.

The Power-On Reset is the result of an RC timing circuit, consisting of Resistor R21 and Capacitor C38.

CECTC* From Pins 1-4 of U36/3. To Pin 16 of U19. The CTC Chip Enable signal from Port Address decoding.

The Manual Reset is generated by a one-shot, flip-flop, one-shot type of circuit to limit the width of the Reset Pulse to approximately 17Ø microseconds. This pulse limit is necessary to avoid suspending refresh to the RAMs, should the Reset happen to occur during the T3 Clock of the M1* cycle of the Op-Code Fetch instruction. This possibility is prevented by synchronizing the Manual Reset circuit to signal "M1*" at Pin 5 of U29.

Without this synchronization, the contents of the RAMs could be destroyed should the Reset Switch be kept closed for too long a period of time.

EIOUT — From Pin 8 of U24. To Pin 14 of the Model II System Bus, where it is labeled "IEOUT" (see same). "IEOUT" is a loop signal of the Z8Ø daisy chain interrupt structure.

The order of interrupt priority on the CPU card is from the CTC U19/2, to the SIO U18/2, and to the DMA U2Ø/1. The PIO on the FDC card is the fourth device of the chain.

Signal "IEOUT" is routed to the PIO on the FDC card at Pin 14 of the Model II System Bus. This signal will be at a logic high when none of the devices on the CPU card is in the process of requesting an interrupt. Refer to Page 2-36 for the Mother Board loop diagram.

Z8Ø DMA Pin 38 — From Pin 11 of U23. To Pin 38 of DMA U2Ø/1 (where it mislabeled as coming from Pin 9 of U23). This is the Interrupt Enable (IEI) signal to the DMA. It is a loop signal of the Z8Ø daisy chain priority interrupt structure. This signal will be at a logic high when neither the CTC nor the SIO is in the process of requesting an interrupt.

Z8Ø DMA Pin 36 — From Pin 36 of U2Ø/1 (where it is mislabeled as going to Pin 11 of U24). To Pin 1 of U24. This is the DMA IEO signal used to create "EIOUT" (see same) at Pin 8 of U24.

KBIRQ* — From Pin 42 of the Model II System Bus. To Pin 2Ø of U19, where it is mislabeled as "KBIRQ". Asserted as the keyboard Interrupt Request from the VDG Board.

INTRQL* From Pin 12 of U19, From Pin 5 of U18, and From Pin 37 of U2Ø/1. The on-board Interrupt Request from the CTC or SIO on Sheet 2 or from the DMA on Sheet 1. To Pin 1 of U4/1, then to the "INT*" (see same) Pin of the CPU. Also used at Pin 4 of U13/3 to set this device, necessary so that a logic low will appear at Pin 1 of U21/3 before the CPU acknowledges the on-board Interrupt Request with signal "INTAK*" (see same).

CLK/TRGØ-2 From Pin 5 of U2/1. To Pins 21-23 of U19. An external 2 MHz Clock signal decrementing the CTC's three programmable Down-Counters.

ZC/TØ-2 CTC zero count/timeout strobes resulting when the CTC Down-Counters reach zero. Used as (baud rate) clocks by the SIO at Pins 13, 14 and 27 of U18.

CESIO* From Pins 5-7,9 of U36/3. To Pin 35 of U18. The SIO Chip Enable signal from Port Address decoding.

RxDA-B To Pins 12/28 of U18. RS232C (serial) data received from Pin 3 of U1Ø (A), and from Pin 11 of U8 (B).

RxCA-B To Pins 13/27 of U18. Receiver clock (baud rate) strobes from CTC ZC/TØ and ZC/T2 outputs.

TxCA-B To Pins 14/27 of U18. Transmit clock (baud rate) strobes from CTC ZC/T1 and ZC/T2 outputs.

SYNCA-B From Pin 8 of U9 (A) and Pin 8 of U8 (B). To U18, Pins 11/29. External device sychronization signals.

CTSA-B From Pin 11 of U9 (A) and Pin 3 of U9 (B). To U18, Pins 18/23. Clear-to-send enables for external logic.

DCDA-B From Pin 3 of U8 (A) and Pin 6 of U8 (B). To U18, Pins 19/22. Data-carrier-detect from external logic.

TxDA-B From Pins 19/26 of U18. To Pins 9/1Ø of U6 (A) and Pins 4/5 of U7 (B). RS232C (serial) data transmitted.

RTSA-B From Pins 17/24 of U18. To Pins 12/13 of U6 (A) and Pins 1/2 of U7 (B). Request-to-send to external logic.

DTRA-B From Pins 16/25 of U18. To Pins 4/1Ø of U7 (A) and Pins 1/2 of U6 (B). Data-terminal ready.

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Glossary - Sheet 1

Only the mnemonics originating from Sheet 1
of the CPU schematic will be covered
under this heading.

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OE*
ROM
(TP 4)

To Pin 2Ø of U11. This is the product Pin description of the EPROM. An input to this Pin by signal "READ*" (see same) is used to control the three-state Data output lines of the EPROM. The Data output lines are normally in the open, or high impedance state. The Data lines will connect to the System Bus whenever signal "READ*" is asserted.

CE*
(TP 3)

To Pin 18 of U11. This is the product Pin description of the EPROM. Input to this Pin by signal "ROMØCE*" is used to power-up the EPROM.

Note: Change U11 on the schematic to indicate that it is a ROM, and not an EPROM. These devices have the same electrical characteristics (see below).

The READ and STANDBY are the two normal modes in which the EPROM/ROM operate.

A READ operation is accomplished by placing logic low signals at the "CE*" (see same) and "OE*" (see same) Pins of the chip. Valid data should appear at the output approximately 3ØØ nanoseconds after Pin "CE*" is made low.

During the READ operation, an EPROM will dissipate approximately 525 milliwatts of power. The power dissipated by a ROM in this same mode will be slightly less.

The EPROM/ROM will switch to the STANDBY mode when Pin "CE*" is made high. The power dissipated by either chip in this "resting" mode will about 25% of their respective READ maximums.

As a special note, Pin "OE*" will lose its control of the Data output lines in the STANDBY mode, because now, the controlling signal has become the high on Pin "CE*". The Data lines will remain in the tri-state mode as long as signal "CE*" is at a logic high.

BUSRQ* (TP 8) — From/To Pin 15 of DMA U2Ø. This is a bi-directional signal which is tied to Pin 17 of the Model II System Bus, and to Pin 25 of the Z8Ø CPU.

As an output signal from DMA U2Ø, to the CPU U12, this is a request signal from the DMA for control of the System Bus. The CPU will grant this request as soon as it completes its current machine cycle by tri-stating its Address, Data, and Control Buses. At this same time, the CPU will also generate signal "BUSAK*" to inform the DMA that the Buses have been released.

During multiple DMA operations, the on-board DMA would use this line as an input to sense when another DMA has sent out a request for control of the System Bus. This action would cause the on-board DMA to refrain from asking for the Bus until the other DMA has completed its operation. Not currently used in Model II.

BAO* — From Pin 13 of DMA U2Ø. This is the Bus Acknowledge Output signal for multiple DMA use. To Pin 16 of the Model II System Bus where it becomes buffered signal "BAKOUT*". Signal "BAO*", along with signal "BAI*" (see same), form a daisy chain for multiple-DMA resolution over Bus control. The on-board DMA (U2Ø) has the highest interrupt priority. Not currently used in the Model II.

CE*DMA — To Pin 16 of DMA U2Ø. This Pin has a dual purpose. It not only functions as the Chip Enable line, but is also programmed to serve as the Wait line to the DMA.

As a Chip Enable function, this line will be asserted when Port F8 (see same) is addressed and becomes signal "CEDMA*" (see same) at Pin 1 of U3. Signal "BUSAK*" (see same) will block this signal at Pin 2 of U3 when the CPU is in the process of granting a bus acknowledge.

Pin 15 of DMA U2Ø functions as a Wait line after the DMA has received a Bus Request Acknowledge from the CPU. This will cause wait states to be inserted in the DMA's operation cycle to slow it down to a speed that matches the Memory or I/O device. The DMA is used in Model II TRSDOS®-based software for Disk-to-Memory and Memory-to-Disk data transfers.

RDY* DMA — To Pin 25 of DMA U2Ø. This is a buffered signal from Pin 41 of the Model II System Bus where it is called "XFERRQ". This signal is monitored by the DMA to determine when the FDC is ready to transfer a byte of data. To state it differently, "XFERRQ" is the transfer request signal from the FDC.

INT* DMA — From Pin 37 of the DMA. To Pin 1 of U4 where it becomes signal "INTRQL*" (see same).

M1* DMA — To Pin 26 of DMA U2Ø. From Pin 27 of the CPU U12. This signal, along with signal "IORQ*" (see same), is used by the DMA as an Interrupt Acknowledge.

IORQ* — From/To Pin 1Ø of DMA U2Ø. This is a bi-directional line. As an input, this signal is part of the Mode 2 interrupt scheme which the Model II supports. With Mode 2 interrupts, the CPU will form a 16-bit Memory Address where the upper 8-bits will be the contents of the CPU's "I" Register, and the lower 8-bits will come from the interrupting device. This Address points to the first two sequential bytes of a table containing the Address of the service routine.

When the DMA is the interrupting device, it will place its special low-byte vector Address on the Data Bus when signals "IORQ*" and "M1*" are both asserted.

Pin 1Ø of DMA U2Ø will become an output line when the DMA has taken control of the System Buses. As an output signal, an asserted "IORQ*" indicates that the lower half of the Address Bus holds a valid Port Address for another I/O device involved in a DMA transfer of data. In this application, it will be one of the Port Addresses such as those of the FDC.

SELECT* — To Pin 2/1 of U39 and to Pin 43 of the Model II System Bus (see same, Sheet 3).

MREQ* DMA	From Pin 12 of the DMA. This signal indicates that the Address Bus holds a valid Address for a Memory Read or Write operation from the CPU. When the DMA has control of the System Buses, this signal indicates that the DMA is requesting a transfer of data to, or from Memory.
RD* DMA	From Pin 9 of the DMA. This is a bi-directional line. As an input line, this signal indicates that the CPU wants to read the Status Bytes from the DMA's Read Registers. This line will become an output after the DMA has taken control of the System Buses. As an output, this signal will indicate a DMA-controlled Read from a Memory or Port Address.
WR* DMA	From Pin 8 of the DMA. This is a bi-directional line. As an input line, this signal indicates that the CPU wants to write Control, or Command Bytes to the DMA Write Registers. This line will become an output after the DMA has taken control of the System Buses. As an output, this signal will indicate a DMA-controlled Write to a Memory or Port Address.
BAI*	To Pin 14 of the DMA. This line is labled "BUSAK*" (see same). This signal, when asserted, is an indication to the DMA that the System Buses have been released for DMA control. See signal "BAO*".
KBINT	Inappropriately shown on Sheet 1, Pin 42 of the Model II System Bus, since it is on Sheet 3 properly labeled as KBIRQ* (see same).
INTRQ* (BUS)	From Pin 11 of the Model II System Bus. To Pin 2 of U4, where it is used to assert an off-board Interrupt from the PIO/FDC, or other add-on devices such as HD, ARCNET, etc. configured in the interrupt daisy chain.
NMIRQ*	From Pin 12 of the Model II System Bus. To Pin 17 of U12. This signal sources from the 30KHz Real Time Clock on the VDG, directing the Z80A to the Real Time Clock Service Routine vectored at 0066H in RAM.
8MHz	From Pin 8 of U30 to Pin 46 of the Model II System Bus for use in pre-comp on the FDC Board. U30 is improperly drawn as a NOR gate: it is a NAND gate.

CPU Board Test Points

TP 1 — From Pin 1Ø of U1/1. This is the 4 MHz System Clock.

TP 2 — From Pin 5 of U2/1. This is a 2 MHz signal used at Pins 21, 22, and 23 of CTC U19/2.

TP 3 — "ROMØCE*".....From Pin 6 of U16/3.

TP 4 — "READ*".....From Pin 8 of U3/3.

TP 5 — "8 MHZ".....From Pin 6 of U3Ø/1.

TP 6 — "CE*".....From Pin 4 of U4/1.

TP 7 — "CLOCK".....From Pin 12 of U1/1.

TP 8 — "BUSRQ*".....From Pin 15 of U2Ø/1.

TP 9 — "CECTC*".....From Pins 1, 2, 3, and 4 of U36/3.

TP 1Ø — "CESIO*".....From Pins 5, 6, 7, and 9 of U36/3.

TP 11 "RESET*".....From Pin 4 of U29/2.

TP 12 "WAIT*".....From Pin 3 of U14/2.

TP 13 "INTAK*".....From Pin 11 of U21/3.

TP 14 This test point is not listed.

TP 15 "SELECT*".....From Pin 11 of U14/3.

TP 16 From Pin 8 of U4/3.

A logic high at this test point is an indication that the Data Drivers of U32/3 and U31/3 are enabled.

TP 17 From Pin 8 of U22/3.

A logic low at this test point is an indication that the Data Receivers of U32/3 and U31/3 are enabled.

TP 18 "ROM*/RAM".....From Pin 8 of U13/2.

CPU Board Port Allocation Table

Port No.	Allocation	Function
FØH	CTC	Channel Ø
F1H	CTC	Channel 1
F2H	CTC	Channel 2
F3H	CTC	Channel 3
F4H	SIO A	Channel A data
F5H	SIO B	Channel B data
F6H	SIO A	Channel A Command/Status
F7H	SIO B	Channel B Command/Status
F8H	DMA	DMA Command/Status
F9H	ROM ENABLE LATCH	ENABLES/DISABLES ROM

CPU Board Jumper Options And Notes

Schematic: The jumper terminals on the schematic are not labeled.

REV A Board: The jumper terminals on this Board are not labeled.

REV B Board: The jumper terminals on this Board are not labeled.

REV C Board: The jumper terminals on this Board are labeled A, B, C, etc. The labels, however, appear only on the later production runs of this Board.

Note: Some of the labeled REV C Boards have labels "A" and "B" referenced to the wrong pads. Refer to the drawing on page 1-21 for the correct pad locations.

REV D Board: The jumper terminals on this Board are labeled EØ, E1, E2, etc. Three jumper options have been deleted from this Board:

1. The 2/4 MHz System Clock option is now permanently wired for a System Clock of 4 MHz. The stake pins at Terminals A and B have been removed, and the terminal pads are now bridged with foil. These pads are not labeled.

2. The 4/8 MHz precomp option is now permanently wired for a precomp of 8 MHz. The stake pins at Terminals U and V have been removed and the terminal pads are now bridged with foil. The pads are still labeled.

3. The SIO Channel B External/Internal Receiver-Transmitter Clock option is now permanently wired to the internal clock sourced from the CTC. The stake pins at Terminals E14 and E15 have been removed, and the terminal pads are now bridged with foil. The pads are still labeled.

CPU Board Standard Jumper Configuration

A - B	4 MHz System Clock.
U - V	8 MHz Precomp Clock.
E7 - E8	SIO Channel A Receive Clock. Sourced from the CTC.
E11 - E12	SIO Channel A Transmit Clock. Sourced from the CTC.
E14 - E15	SIO Channel B Receive/Transmit Clock. Sourced from the CTC.

CPU Board Jumper Configuration For BISYNC Operation

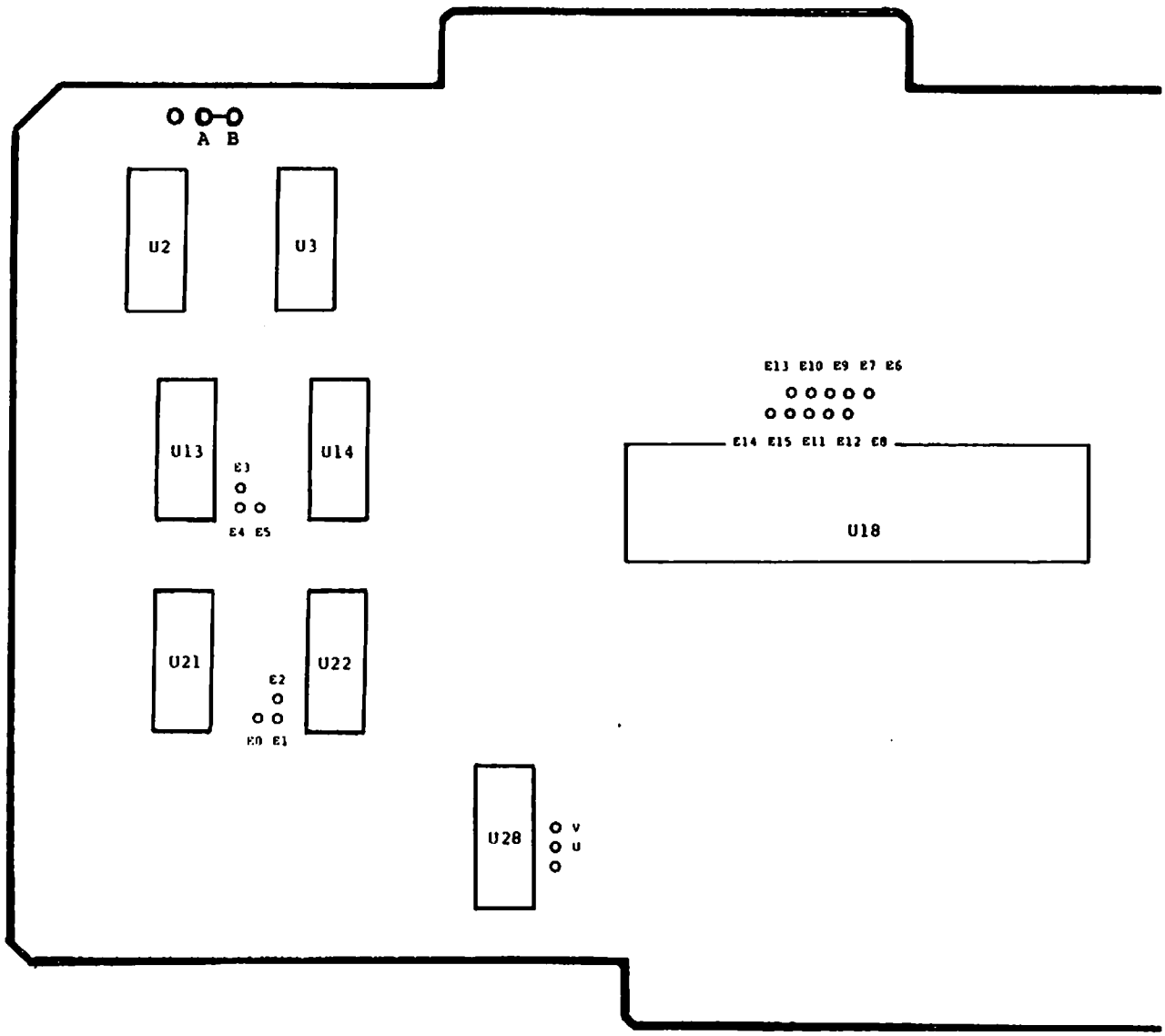
Note: The CPU Board must be modified for BISYNC operation. Refer to Model II Technical Bulletin II:17 for the modification procedure.

E6 - E7	SIO Channel A Receive Clock. Sourced from external device.
E1Ø - E11	Channel A Transmit Clock. From CTC to external device.
E9 - E12	SIO Channel A Transmit Clock. Sourced from external device.

Jumper Terminal Cross Reference
REV C and REV D CPU Boards

REV C	REV D	Source/Destination
N	EØ	From Pin 8 of U21/2.
P	E1	To Pin 4 of U14/2.
M	E2	From R12. +5 volt pull-up
S	E3	From Pin 9 of U13/2.
T	E4	To Pin 5 of U22/2 and Pin 1Ø of U21/2.
R	E5	From R1Ø. +5 volt pull-up
L	E6	From Pin 11 of U1Ø/2.
J	E7	To Pin 13 of U18/2.
K	E8	From Pin 7 of U19/2.
H	E9	From Pin 8 of U1Ø.
F	E1Ø	To Pins 12 and 13 of U7/2.
G	E11	From Pin 8 of U19/2.
I	E12	From Pin 14 of U18/2.
D	E13	From Pin 6 of U9/2.
C	E14	From Pin 9 of CTC U19/2.
E	E15	To Pin 27 of SIO U18/2.
A	A	To Pin 3 of U2/1.
B	B	From Pin 9 of U28/1.
U	U	To Pin 9 of U3Ø/1.
V	V	From Pin 8 of U29/1.

CPU Board Jumper Terminal Locator



The physical location of the jumper terminals illustrated above are identical for all Board revisions.

The labels shown are those of the REV D Board.

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Section Two

Model II FDC Board - Early

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Contents

The listings in this glossary are divided into 2 sections, respective to the 2 sheets of the Early FDC Board schematic.

When a signal from one sheet is referenced to another, a pointer, "/#", will be used to indicate the sheet: i.e. From Pin 9 of U14/2 To Pin 24 of U6/1.

REV D is the last revision of the old style FDC Board. The schematics contained in the manual reflect the circuits which are on the REV C Board. Some of the circuits changes between the different old style FDC Boards will be pointed out in the glossary.

Index for Early FDC Board Signals

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Glossary - Sheet 1

Only the mnemonics originating from Sheet 1 of the Early FDC schematic will be covered under this heading.

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XF* From Pin 8 of U2Ø. This signal decodes the low-order address nibble as FH when AØI-A3I are all logic high. "XF*" goes to Pin 12 of U8, where it is NANDed with signal "E8*-EF*" to produce signal "EF*" (see same). Pins 6/8 of U2Ø are shown reversed on the schematic.

EX* From Pin 6 of U2Ø. This signal decodes the upper address nibble, or first half of the FDC Port Addresses, as EH to access Ports EØ-EF. See page 2-5 for a functional summary of Ports allocated to the FDC Board.

Signal "EX*" is used at Pin 9 of U19 and Pin 1 of U8. U8 and U19 are used as steering gates for signal "EX*", and are controlled by the logic status of Address line A3. When Address line A3 is a logic high, "EX*" will be steered through U19 to produce signal "E8*-EF*" (see same). Conversely, when Address line A3 is at a logic low, "EX*" will be steered through U8 to produce signal "EØ*-E7*" (see same).

E8*-EF* From Pin 8 of U19. This signal will be asserted when the CPU is in the process of accessing Ports E8 through EF. "E8*-EF*" is applied to Pin 13 of U8 where it is NANDed with "XF*" to produce signal "EF*" (see same).

EØ*-E7* From Pin 3 of U8. This signal will be asserted when the CPU is in the process of accessing Ports EØ-E7.

"EØ*-E7*" is used at:

* Pin 9 of U8 where it is NANDed with a logic low Address A2 to produce signal "CEPIO*" (see same). Signal "CEPIO*" will be asserted when the CPU is in the process of accessing Ports EØ through E3.

* Pin 4 of U8 where it is NANDed with a logic high Address A2 to produce signal "CEFDC*" (see same). Signal "CEFDC*" will be asserted when the CPU is in the process of accessing Ports E4 through E7.

* Pin 5 of U19 where it is NANDed with an asserted signal "IN*" to produce a logic low at Pin 6.

  Pin 6 will be at a logic low only when the CPU is in the process of performing a Read operation at Ports EØ through E7. During this Read operation, the logic low appearing at Pin 6 will be ORed through U1Ø, then inverted at Pin 8 of U18 to produce signal "CPUIN" (see same). "CPUIN" is used to enable the Data Drivers of U32 and U33.

  Note: The output of U1Ø (Pin 6) is also used at Pin 5 of U11/2 where it is ANDed with signal "CEPIO*" to enable the Data Drivers of U12 and U23. This additional output from Pin 6 of U1Ø is not shown on the schematic.

* Pin 1Ø of U1Ø, where it is ORed through to appear at Pin 9 of U21. Pin 1Ø of U21 will be at a logic low whenever the CPU is in the process of accessing any Port. The logical product of the two inputs to U21 will be used to control the logic status of signal "SELECTI*" (see same). In this application, "SELECTI*" will be asserted only when the CPU is in the process of performing a Read/Write operation at Ports EØ through E7.

EF* From Pin 11 of U8. This signal will be asserted when the CPU is in the process of accessing Port EF.

"EF*" is used at Pin 5 of U21 where it is NANDed with signal "OUT*" (see same) to produce signal "DRVSLT*" (see same). Signal "DRVSLT*" will be asserted only when the CPU is in the process of performing a Write operation at Port EF.

Signal "EF*" is also used at Pin 9 of U1Ø where it is ORed with EØ*-E7* (see same) to appear at Pin 9 of U21. Pin 1Ø of U21 will be at a logic low whenever the CPU is in the process of accessing any Port.

The logical product of Pins 9 and 1Ø of U21 will be used to control the status of signal "SELECTI*" (see same). In this application, "SELECTI*" will be asserted only when the CPU is in the process of performing a Write operation to Port EF.

PORT #	ALLOCATION	FUNCTION
EØH	PIO Port A – Data	Printer and FDC INT. status
E1H	PIO Port B – Data	Printer Data (output)
E2H	PIO Port A – Control	Configuring Port A
E3H	PIO Port B – Control	Configuring Port B
E4H	FDC Status/CMD Register	FDC Status and CMD
E5H	FDC Track Register	Current Track Add.
E6H	FDC Sector Register	Current Sector Add.
E7H	FDC Data Register	Data To or From Diskette
EFH	Drive Select Latch	Drive, Mode, Side Select

CEPIO* (TP 18) From Pin 8 of U8. To Pin 4 of PIO U22/2. This is Chip Enable signal for the PIO.

The PIO will be selected when this signal is at a logic low. This selection will allow the CPU to communicate with the PIO. Communication with this chip will be in progress when the CPU is addressing Ports EØ through E3. The functional allocation of each of these Ports is listed above.

"CEPIO*" is also used at Pin 6 of U11/2 where it is ANDed with the logic low at Pin 5. Pin 5 of U11 will be at a logic low when the CPU is in the process of performing a Read operation at Ports EØ through E7. The result of this input combination will cause the Data Drivers of U12/2 and U23/2 to be enabled only when the CPU is in the process of performing a Read operation at PIO Ports EØ through E3.

CEFDC* (TP 14) From Pin 6 of U8. To Pin 3 of FDC U6. This is the Chip Enable signal for the FDC.

The FDC chip will be selected when this signal is at a logic low. This selection will allow the CPU to communicate with the FDC. Communication with this chip will be in progress when the CPU is addressing Ports E4 through E7. The functional allocation of each of these Ports are listed on Page 2-5.

DRVSLT* From Pin 6 of U21. Signal "DRVSLT*" will be asserted only when the CPU is in the process of performing a Write operation to Port EF.

"DRVSLT*" is used at Pin 9 of U17 to latch the logic status of the following signals.

* Drive Select.

  A logic high at Pin 2, 5, 7, or 1Ø of U17 will select one of four drives: "DS1*", "DS2*", DS3*", or "DS4*". Only one of these signals should be asserted at any one time.

* Side Select.

  A logic high at Pin 15 of U17 will select Side Ø of the diskette. Signal "SDSEL" at Pin 8 of U16 will be at a logic low with this selection.

* Double Density Select.

  A logic low at Pin 12 of U17 will select the Double Density mode. This signal is labeled "FM/MFM*" (see same), and goes to "3Ø Pin 1 U29 Pin 1Ø, and U6 Pin 37.

SELECTI* From Pin 8 of U21. This signal will be asserted when the CPU is in the process of performing a Read/Write operation at Ports EØ through E7, and EF.

"SELECTI*" is routed to Pin 3 of U34/2, then further to Pin 43 of the Model II System Bus.

Note: This signal is produced by all of the original Model II Boards (this excludes the revised FDC Board). Each Board has this signal tied to Pin 43 of the Model II System Bus (wired AND). "SELECTI*" is not used, and it's intended purpose is unknown. It functions as a "Board Busy" signal, since it is activated only when the CPU is in the process of performing a Memory Read/Write or I/O operation.

CPUIN — From Pin 8 of U18. This signal will be asserted when the CPU is in the process of performing a Read operation at Ports EØ through E7. "CPUIN" will also be asserted when the CPU is in the process of servicing an Interrupt Request from the PIO.

"CPUIN" is applied to Pins 1 and 15 of U32/2 and U33/2. The logic high at Pins 1 and 15 is used to enable the Data Drivers of these bi-directional Buffers.

WRITEI* — From Pin 18 of Buffer U36. This signal will be asserted when the CPU is writing to a Memory Address or an I/O Port.

"WRITEI*" is used at Pin 1 of U21 where it is NANDed with "IOCYCI*" to produce signal "OUT*" (this signal is not labeled).

IOCYCI* — From Pin 16 of Buffer U36. This signal will be asserted when the CPU is writing or reading any I/O Port. "IOCYCI*" will also be asserted when the CPU is acknowledging an Interrupt Request.

"IOCYCI*" is used as outlined below.

* At Pin 2 of U21 where it is NANDed with "WRITEI*" to produce "OUT*" (see same). "OUT*" is not labeled.

* At Pin 13 of U21 where it is NANDed with "READI*" to produce "IN*" (see same). "IN*" is not labeled.

* At Pin 2 of U19 where it is NANDed with "SYNCI*" to produce "INTAK*" (see same).

* At Pin 36 of PIO U22/2 where it is called "IORQ*" (see same).

READI* — From Pin 5 of Buffer U36. This signal will be asserted when the CPU is performing a Read at any Memory Address or I/O Port. It is NANDed at Pin 12 of U21 with signal "IOCYCI*" (see same) to produce signal "IN*" (see same). Signal "READI*" is also used at Pin 35 of PIO U22/2 where it is called "RDI*" (see same).

SYNCI* From Pin 3 of Buffer U36. "SYNCI*" is the M1* signal produced by the CPU during an Op-code Fetch cycle, or an Interrupt Acknowledge.

"SYNCI*" is used at Pin 1 of U19 where it is NANDed with "IOCYCI*" to produce signal "INTAK*" (see same).

"SYNCI*" is also used at Pin 1 of U1Ø/2 where it is ORed with "RESETI*" to Pin 37 of U22/2. The signal at Pin 37 of the PIO is called "M1*" (see same).

RESETI* From Pin 14 of Buffer U36. This is the System Reset signal which is initiated during a Power On or Manual Reset cycle.

"RESETI*" is used at Pin 19 of FDC U6 where it is called "MR*" (see same).

Signal "RESETI*" is applied to Pin 1 of U17 where it is used to clear the outputs of this latch. Note: The "CLR" input to U17 is Pin 1. Label it. Also, the Pin 1 input should show an inversion bubble: draw it in.

"RESETI*" is also used at Pin 2 of U1Ø/2 where it is ORed with "SYNCI*" to Pin 37 of U22/2. The signal at Pin 37 of the PIO is called "M1*" (see same).

8MHZI (TP 17) From Pin 9 of U36. This is the 8 MHz clock from the CPU Board. It is used at Pin 9 of U1 to clock through the logic status of signal "WD" (see same).

Note 1: The four parts of U1 are wired as a shift register which is clocked at 8 MHz. This arrangement provides a predictable 125 nanosecond delay per stage for the logic high of "WD" appearing at Pin 4 of U1. U1 is part of the Write Precompensation logic.

The three delayed outputs of U1 are used at U2 along with the "EARLY" and "LATE" signals from Pins 11 and 8 of U7. The logical result of this combination will produce write precompensated signals at Pins 7 and 9 of U2. The Write Precompensated pulses appearing at Pin 7 of U2 will have a 125 nanoseconds shift, and those at Pin 9, a 25Ø nanosecond shift.

Note 2: The steering logic consisting of four parts of U3 is programmed to allow only the 25Ø precompensated pulses to pass through to One-Shot U37. This steering is controlled by the position of Jumpers 6, 7, and 8. The normal System configuration is to have 6 and 7 jumpered for 25Ø precompensation. The jumper between 7 and 8 shown on the schematic is incorrect.

Note 3: The precompensated write pulse appearing at Pin 1 of U3 is used as a trigger at Pin 1Ø of One-Shot U37. The purpose of this one-shot is to ensure that the pulse width of the write data pulses will always be at approximately 25Ø nanoseconds. This output pulse is inverted at Pin 4 of U16 (TP 1Ø) to become signal "CWD" (see same).

Note 4: U37 mentioned in Note 3, appeared as a wired mod, or as a piggyback module on the Rev Blank, A, and B Boards. The Rev C and D Boards have this one-shot circuit incorporaed into the Board design.

IN* From Pin 11 of U21. This signal is not labeled on the schematic. "IN*" is the logical product of signals "READI*" and "IOCYCI*", and it will be asserted when ever the CPU is in the process of reading any I/O Port Address.

"IN*" used at Pin 4 of U19 where it is NANDed with "EØ*-E7*" to produce a logic low at Pin 6 of U19. This low at Pin 6 is ORed through U1Ø, then further, to be inverted at Pin 8 of U18 to become signal "CPUIN" (see same).

When signal "IN*" is asserted, the logic low appearing at Pin 6 of U1Ø is also used at Pin 5 of U11/2. If "CEPIO*" is asserted at Pin 6 at this same time, the logical product of these two signals will enable the Drivers of U12/2 and U23/2 for a CPU Read of the PIO.

Note 1: The signals of the Address and Data lines of the Model II System Bus travel between the Boards in inverse logic: i.e., a logic high on a Board will appear as a logic low on the Bus.

Note 2: Buffers U12 and U23 mentioned above are electrically wired between the internal Data Bus of the FDC Board and the Data Input/ Output lines of the PIO. These Buffers are used to invert the logic levels of the data going to, and coming from the PIO chip. This correction is necessary because the internal data Bus of the FDC Board is wired for inverse logic.

Signal "IN*" is also ORed with "OUT*" through U1Ø, then appears at Pin 1Ø of U21 where it is NANDed with the FDC Port signals "EØ*-E7*" or "EF*" to generate signal "SELECTI*" (see same).

"IN*" is used again at Pin 4 of FDC U6 where it is called "RE*". This is the Read Enable signal to the FDC chip. A logic low at this input will cause the FDC to gate out data from a selected Register when the Chip Select signal at Pin 3 is at a logic low.

OUT* From Pin 8 of U21. This signal is not labeled on the schematic.

"OUT*" is the logical product of signals "WRITEI*" and "IOCYCI*", and it will be asserted when ever the CPU is in the process of writing to any I/O Port Address.

Signal "OUT*" is used as follows.

* At Pin 4 of U21 where it is NANDed with "EF*" to produce signal "DRVSLT*" (see same).

* At Pin 12 of U1Ø where it is ORed with "IN*" to appear at Pin 1Ø of U21. It is NANDed with "EØ*-E7*" or "EF*" to generate signal "SELECTI*" (see same).

* At Pin 2 of FDC U6 where it is called "WE*". This is the Write Enable signal to the FDC chip. A logic low at this input will allow the CPU or DMA to gate in data into the selected Register when the Chip Enable signal is asserted at Pin 3.

INTAK* From Pin 3 of U19. This signal is the logical product of "SYNCI*" and "IOCYCI*", which are M1* and IORQ* on the CPU Board. It will be asserted when the CPU is in the process of servicing, or acknowledging an Interrupt Request.

In this application, the NANDed result of "INTAK*", "IEIN" (see same), and "IEOUT" (see same) through U13 will be used to enable the Data Drivers of U12/2, U23/2, U32/2, and U33/2.

Note: The logic high at Pin 2 of U13 is an indication that a device of higher priority has not generated an Interrupt Request. The logic high on Pin 13 of U13, on the other hand, is an indication that the PIO has generated an Interrupt Request. From this we can see that the Drivers mentioned above will only be enabled when the Interrupt Request of the PIO is in the process of being serviced by the CPU.

IEIN — From Pin 13 of the Model II System Bus. To Pin 2 of U13 and Pin 24 of the PIO. For a functional understanding of this signal refer to the note under "INTAK*" and also to the diagram on page 2-36.

IEOUT — From Pin 14 of the Model II System Bus. To Pin 5 of U16 and Pin 22 of the PIO. For a functional understanding of this signal refer to the note under "INTAK*" and also to the diagram on page 2-36.

TG43 — From Pin 29 of FDC U6. This signal will be asserted between Tracks 44 through 76 in the Double Density or Single Density modes.

"TG43" is inverted at Pin 6 of U16, then onward to Pin 2 of the Drive Bus. "TG43" is used to reduce the write current of the drive by approximately 25% when the head is positioned between tracks 44 through 76. The peak-to-peak write current for an 8-inch drive before Track 44 is about 1Ø milliamperes.

Signal "TG43" is also used at Pin 5 of U7 where it is ANDed with "FM*/MFM" (see same) to enable two parts of U7. The enabling of these gates will allow the "EARLY" (see same) and "LATE" (see same) signals to pass through to U2 for Write Precompensation.

Note 1: When the drive head is positioned on a track less then 43, "TG43" will be negated and block the "EARLY" and "LATE" signals at Pin 5 of U7.

Note 2: During the time that "TG43" is negated, the Write Data will be sourced from Pin 7 of U1.

FM/MFM* From Pin 12 of U17. This is the Density Mode Enable signal. A logic low will enable the Double Density mode. This mode will be selected when the CPU does a Write to Port EF with data bit 7 at Pin 13 of U17 at a logic low.

When the Double Density mode is selected, "FM/MFM*" will be used as indicated below.

* At Pin 37 of FDC U6. A logic low at this input will set the interface logic of the FDC and enable the Double Density circuits of the chip.

* At Pin 4 of U7 where it is ANDed with "TG43" to gate through the precompensation signals "EARLY" and "LATE" to U2. See "TG43" for supporting information.

* At Pin 1Ø of U29 where it is used to disable the Single Density mode 5ØØ KHz signal at Pin 9. Refer to the second note below.

* At Pins 1 and 2 of U3Ø where it is inverted at Pin 3 to place a logic high at Pin 5 of U3Ø. Refer to the second note below.

  The low at Pins 1 and 2 of U3Ø is also used to turn on Transistor Q2. Q2 will place Potentiometer R37 in parallel with Potentiometer R36.

  Note 1: Potentiometers R36 and R37, along with Potentiometers R32 and R5, should be adjusted only as outlined in the FDC Board alignment procedure, FDCALG.

  Note 2: The two parts of U29 will divide the 2 MHz VCO signal appearing at Pin 6 of U27, by 2 and by 4, respectively. The 1 MHz signal at Pin 5 of U29 will appear at Pin 8 of U3Ø when the Double Density mode is enabled (this is due to the low on Pin 1Ø of U29 and the high on Pin 5 of U3Ø). When the Single Density mode is enabled, Pin 1Ø of U29 will be high and Pin 5 of U3Ø low

and the 5ØØ KHz signal now appearing at Pin 9 of U29 will be routed through to Pin 8 of U3Ø.

The signals (SD=5ØØ KHz, DD=1 MHz) at Pin 8 of U3Ø are used at U28 of the Clock Recovery circuit.

The signals at Pin 8 of U3Ø will be divided again at Pin 5 of U14 to become the nominal Clock Recovery frequencies (DD= 5ØØ KHz, SD=25Ø KHz) for the FDC through U4 and U7.

WG — From Pin 3Ø of FDC U6. This is the Write Gate signal to the drive. "WG" will be set to a logic high approximately 2 microseconds before an actual Write operation in the FM mode. In the MFM mode, it will be set to a logic high approximately 1 microsecond before the actual Write.

The Write Gate signal is inverted at Pin 12 of U4 to become signal "WG*". "WG*" is tied to Pin 4Ø of the Drive Bus.

DIR — From Pin 16 of FDC U6. This is the Head Direction to the Drive logic. "DIR" works in conjunction with signal "STEP" (see same). Signal "STEP" will position the head inward, or towards Track 76 when "DIR" is at a logic high, and will position the head outward, or towards Track Ø, when "DIR" is at a logic low. The direction signal will appear on the Drive Bus approximately 12 microseconds before the first step pulse is executed.

The direction signal is inverted at Pin 12 of U5 to become signal "DIR*". "DIR*" is tied to Pin 34 of the Drive Bus.

STEP — From Pin 15 of FDC U6. This is a 2 microsecond positive-going pulse, used to move, or position the drive head over the diskette media. For every step pulse executed by the FDC, the drive head will move one track location in the direction determined by the logic status of signal "DIR" (see same). The first step pulse will appear approximately 12 microseconds after signal "DIR" becomes asserted.

The step pulse is inverted at Pin 2 of U4 to become signal "STEP*" (TP 12). "STEP*" is tied to Pin 36 of the Drive Bus.

WPRT* From Pin 44 of the Drive Bus. To Pin 36 of FDC U6.

"WPRT*" is the Write Protect signal from the drive. The Write Protect signal is used by the FDC to determine if the diskette in use is write protected. The status of this input signal will be sampled whenever the FDC receives a write command. A logic low at this input will set the write protect bit (bit 6) in the Status Register of the FDC.

IP* From Pin 2Ø of the Drive Bus. To Pin 35 of FDC U6.

"IP*" is the Index Pulse from the drive. It is used to inform the FDC chip when the index hole is encountered on the diskette. This pulse should appear every 166.67 milliseconds after the drive spindle has come up to speed. The Index Pulse is used in the FDC to synchronize various command operations. Refer to the FD179x spec sheet for the details on how this signal is used.

TRKØ* (TP 4) From Pin 42 of the Drive Bus. To Pin 34 of FDC U6. This is the Track Ø signal. A logic low at this input is used to inform the FDC that the drive head is positioned over Track Ø.

WD From Pin 31 of FDC U6.

"WD" is the Write Data Pulse signal to the drive. The Write Data is a serial train of bits representing address marks as well as data and clock information in both the FM and MFM formats. Each bit of the pulse train will be made up of 2ØØ nanosecond pulses (for DD) or 5ØØ nanosecond pulses (for SD).

"WD" is used at Pin 4 of U1. The four parts of U1 are wired as a Shift Register. The output stages will introduce delays of 125, 25Ø, 375, and 5ØØ nanoseconds. These delays are used as outlined on the next page.

* Pin 7 of U2. The "125" shift.

  The input signals to U2 for the "125" are:

  1. Pin 2 of U1. This is the 125 nanosecond delay, and it is used as the NOMINAL Write Data signal.

  2. Pin 4 of U1. This is the zero delay, and it is used as the EARLY Write Data signal.

  3. Pin 7 of U1. This is the 25Ø nanosecond delay, and it is used as the LATE Write Data signal.

* Pin 9 of U2. The "25Ø" shift.

  The input signals to U2 for the "25Ø" are:

  1. Pin 7 of U1. This is the 25Ø nanosecond delay, and it is used as the NOMINAL Write Data signal.

  2. Pin 4 of U1. This is the zero delay, and it is used as the EARLY Write Data signal.

  3. Pin 15 of U1. This is the 5ØØ nanosecond delay, and it is used as the LATE Write Data signal.

The Nominal and/or Precompensated Write Data bits appearing at Pin 1 of U3 can be sourced from Pin 7 of U2 (with Terminals 7 and 8 jumpered for the 125 nanosecond shift) or from Pin 9 of U2 (with Terminals 6- and 7 jumpered for the 25Ø nanosecond shift). See signals "CWD" and "8MHZI" for supporting information.

RDY — To Pin 32 of FDC U6. This input to the FDC chip is used to indicate the readiness of the disk drive. This signal must be at a logic high before any of the read or write commands to the FDC can be executed. There are some exceptions: see signal "MR*", also, the spec sheet on the FD179x.

The exact variables involved to produce this signal will depend on the type of drive in use. A few of the things a drive COULD check before producing this signal are listed on the next page.

* Check if the drive is selected.

* Check that the drive door is closed.

* Check to see if the drive spindle is up to speed.

* Check for the presence of the diskette Index Pulse.

"RDY" is the inverted result of the Ready signal appearing at Pin 22 of the Drive Bus.

HLD* (TP 21) — From Pin 1Ø of U4. This signal is the inverted result of signal "HLD" at Pin 28 of FDC U6.

"HLD*" is used to control the loading of the drive head against the diskette media. The drive head is loaded when this signal is asserted at a logic low.

The "HLD*" signal is tied to Pin 18 of the Drive Bus. The negative-going edge of this signal is also used as a trigger at Pin 1 (label it!) of One-Shot U31. This one-shot is used to keep signal "HLT" (see same) negated for a period of approximately 75 milliseconds (the range specified in the service manual is 5Ø to 1ØØ milliseconds).

Signal "HLD*" is also used at Pin 1 of U16, which is part of the Raw Read Data Enable logic. Refer to signal "READ DATA" to see how this logic is enabled.

HLT — To Pin 23 of FDC U6. This is the Head Load Timing signal to the chip. The FDC chip will assume that the drive head is loaded, or engaged when this input signal switches to a logic high.

The initialization of this signal will be delayed with respect to the negative-going asserted edge of signal "HLD*" by approximately 75 milliseconds. One-Shot U31 will introduce this delay whenever it is triggered by "HLD*". This delay is necessary to allow the drive head to settle, or engage completely before the FDC does an actual Read or Write operation to or from the diskette media. See note on the next page.

Note: The Head Load Timing is a drive specification. The head engagement time for most drives will fall between the range of 30 to 100 milliseconds. U31 is used to set the HLT to an average of approximately 75 milliseconds.

"HLT" is also used at Pin 4 of U13. U13 is part of the Raw Data Read Enable logic. Refer to signal "READ DATA" to see how this logic is enabled.

Note: The FDC will be able to read or write to the diskette only when signals "HLD" and "HLT" are true at Pins 28 and 23 of the FDC chip.

Pin 1 of FDC U6.

This Pin is not indicated on the block symbol of FDC, U6. Add the following to your schematic.

From the top of the block symbol, draw a zener diode symbol with its cathode end connected to ground. The anode of this zener should be shown tied to Pin 1 of the chip. This is a 2.7 volt zener.

Note 1. According to the FD179x spec sheet, Pin 1 is internally connected to a back bias generator and should be left open. However, in the early days of the Model II, it was found that the FDC chip would become thermal at times. The problem was eventually isolated to the voltage at Pin 1: it was becoming too negative. The zener modification was introduced as a correction by clamping the voltage at Pin 1 to minus 2.7 volts. This zener should appear on the foil side of the Rev Blank, A, and B Boards. The Rev C, and D Boards have this zener (CR1) incorporated into the Board design.

Note 2. When disk I/O problems are being encountered, don't hesitate to hook a scope probe to Pin 1 of the FDC chip. What you see there could tell you a lot about the chip. Make sure that the DC voltage level at this Pin is at minus 2.7 volts. Also, this voltage level should be clean, free of RF noise, or spikes. Don't guesstimate, just replace the FDC chip if it appears noisy.

MR* To Pin 19 of FDC U6. This is the Master Reset input to the FDC chip. A logic low will reset the FDC chip. A RESTORE (Ø3H) will be loaded into the Command Register, and the Not Ready Status bit will be reset during this time. The RESTORE command will be executed when this input returns to a logic high.

"MR*" is controlled by signal "RESETI*" (refer to this signal for supporting information) from Pin 14 of U36.

CLK (TP 13) To Pin 24 of FDC U6. This is the 2 MHz Master Clock input which is used by the chip as an internal timing reference.

The source of this input is labeled "OPTION PIN B" which originates from Terminal B on sheet 2 of the schematic. In the normal System configuration, Terminal B should be jumpered to Terminal A as indicated on the schematic. Refer to signal "CLOCKI" for supporting information.

RCLK (TP 23) From Pin 3 of U7. To Pin 26 of FDC U6.

"RCLK" is used as the Data Recovery signal by the FDC. The nominal "RCLK" frequency is 5ØØ KHz in the Double Density mode, and 25Ø KHz in the Single Density mode.

The two parts of U4 at the input to the FDC are used to decrease the duty cycle of the recovery clock by a slight percentage. This correction was probably done to compensate for the slight propagational delay introduced by U14 (at Pin 5). Note that the signals preceeding U14 are used for the actual clock recovery correction.

The basic function of the resultant "phase corrected", or adjusted "RCLK" is to latch in the read data input bits appearing at Pin 27 of the FDC. Refer to signals "FM/MFM*", "READ DATA", and "RAW DATA" for supporting information.

DRQ (TP 15) From Pin 38 of FDC U6. This is the Data Request signal from the FDC.

"DRQ" in normally kept at a logic low. It will be pulled to a logic high by Resistor R1Ø when the Data Register of the FDC contains assembled data during a Read operation, or when the Data Register is

empty during a Write operation. The data request signal will switch back to a logic low after the DMA services the FDC by reading or loading the Data Register.

Signal "DRQ" is tied to Pin 11 of U34/2 where it is buffered at Pin 1Ø to become signal "XFERRQ". Note: Change "XFERRQI*" at Pin 11 to "XFERRQI".

Signal "XFERRQ" is routed to Pin 41 of the Model II System Bus where it will travel back on the same Bus to Pin 41 of the CPU Board. "XFERRQ" is applied directly to Pin 25 of the DMA chip on the CPU Board. Pin 25 is the READY input to the DMA.

Note: Most data transfers from Drive-to-Memory or Memory-to-Drive are handled by the DMA. The DMA is used because its data transfer speed is much faster than the CPU.

The DMA can be programmed to operate in any of three modes: Byte, Burst or Continuous. The Byte mode is used for all DMA data transfers in the Model II. In this mode, the DMA and CPU will alternately share the System Bus during data transfer operations to and from the FDC. The time sharing of the System Bus during this period is called "interleaving". Interleaving allows the CPU to continue with its monitoring functions of the System.

The "XFERRQ" signal at Pin 25 of the DMA will be continuously monitored by this device to determine when the drive is ready for a read or write operation. When "XFERRQ" is asserted, the DMA will ask the CPU for control of the System Bus by generating signal "BUSRQ*". Signal "BUSAK*" is used to inform the DMA that the CPU has relinquished control of the System Bus.

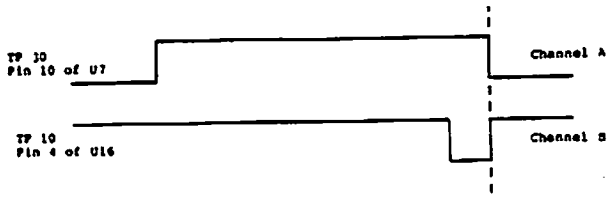
INTRQ (TP 13) — From Pin 39 (label it!)of FDC U6. This is the Interrupt Request signal from the FDC chip. It is normally kept at a logic low. It will be pulled to a logic high by Resistor R14 at the completion of any command. It will switch back to a logic low after the Status Register is read, or the Command Register is written to.

"INTRQ" is tied to Pin 15 of PIO U22/2. Pin 15 is Bit Ø of the "A" Port of the PIO. The PIO is programmed to monitor the logic status of this bit. The PIO will generate an Interrupt Request to the CPU when the logic status of this bit switches to a logic high. The CPU will service this Interrupt Request (under the conditions outlined by signal "INTRQI*") by executing a Read operation to Port EØ. The Status of all of the input lines of the PIO's "A" Port will be checked during this read. When this Read operation is in progress, the logic high of Bit Ø will inform the CPU that the FDC chip has generated an Interrupt Request. Upon completion of this Read to Port EØ, the CPU will perform another Read operation, but this time to Port E4 to check the bit levels of the FDC's Status register. The meaning of the Status bits in this Register will be a function of the type of command previously executed by the FDC.

EARLY — From Pin 17 of FDC U6. This is the early signal for Write Precompensation. When this signal is asserted along with the Write Data pulse appearing at Pin 31, signal "EARLY" will place a high at Pin 13 of U7. Pin 12 of U7 should already be at a high by the "FM*/MFM" and "TG43" signals. The resulting high at Pin 14 of U2 will route the 1Cl input signal to the Pin 7 output and 2Cl input signal to the Pin 9 output. The signal appearing at Pin 7 will be the early precompensated write bit for the "125" mode: that at Pin 9 will be the same, but for the "25Ø" mode. See signals "WD" and 8 MHZI" for supporting information.

LATE — From Pin 18 of FDC U6. This is the late signal for Write Precompensation. When this signal is asserted along with the Write Data pulse appearing at Pin 31, signal "LATE" will be used as a trigger at Pin 1Ø of of One-Shot U31. The one-shot will produce a positive-going pulse at Pin 5 (label this output line TP 3Ø) when triggered. The width of the pulse will depend on the setting of Potentiometer, R5. Potentiometer R5 should be adjusted as outlined in the FDCALG procedure.

The waveforms associated with the R5 adjustment are illustrated on the next page. The pulse at TP 3Ø should have a period of approximately 2.5 microseconds after the R5 adjustment.



The positive pulse at Pin 5 of the one-shot will place a high at Pin 1Ø of U7. Pin 9 of U7 should already be at a high by the "FM*/MFM" and "TG43" signals. The resulting high appearing at Pin 2 of U2 will route the 1C2 input signal to the Pin 7 output and the 2C2 input signal to the Pin 9 output. The signal appearing at Pin 7 will be the late precompensated write bit for the "125" mode: that at Pin 9 will be the same, but for the "25Ø" mode. See signals "WD" and "8 MHZI" for supporting information.

CWD (TP 1Ø) — From Pin 1Ø of U4. This is the Compensated Write Data signal. A write bit transition will appear as a negative-going 25Ø nanosecond pulse. One-Shot U37 was added to the circuit to keep the widths of the write data bits consistent.

"CWD" is tied directly to Pin 38 of the drive Bus.

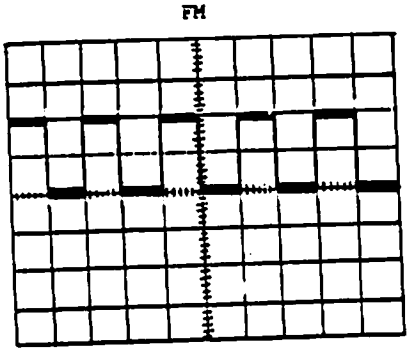
Note: Two types of FDC chips are used on this Board, the FD1791-Ø2 from Western Digital, and the SY1791-Ø2 from SYNERTEK.

The SY1791-Ø2 is a second source for the FD1791-Ø2. When it was introduced, problems with formatting past 43 began to appear. The cause was isolated to the EARLY pulse: it was ending sooner than the EARLY pulse of the FD1791-Ø2. This early termination caused double pulses to appear on the Compensated Write Data. To correct this problem, a modification was made by tying the Write Data out (TP 1Ø) to the Reset (Pin 1) of the shift register. This circuit addition allows the bit transition of the Write Data to clear the Shift Register, thus preventing double data pulse generation.

READ DATA — From Pin 46 of the Drive Bus. This is the Raw Read Data from the drive. It will be gated through to Pin 6 of U13 (TP 9) only when the drive head is loaded and when the Head Load Timing delay has run out. This gating prevents the possiblity of reading garbage before the head has had time to settle on the diskette media. See signals "HLD*" and "HLT" for supporting information.

RDA (TP 24) — From Pin 13 of One-Shot U25 (label it!). This is the Raw Data Adjusted signal.

In the Single Density mode, a 2F pattern scoped at Pin 13 should display a 5ØØ KHz square-wave as illustrated by the diagram below. Potentiometer R36 is used to set the duty cycle at 5Ø%. This adjustment is outlined in the FDCALG procedure.

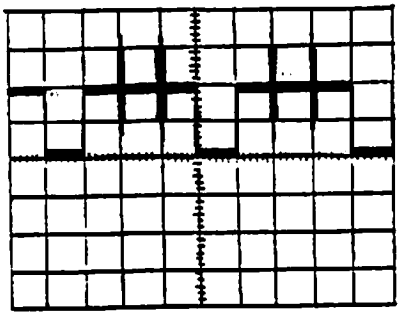


Timebase 1 usec/div
Channel A 2 V/div
Adjust for 50% duty cycle

The waveform of signal "RDA" in the Double Density mode is illustrated on the next page. Potentiometers R32 and R37 should be used to minimize the glitches.

Note: The settings of Potentiometers R5, R32, R36, and R37 are described in the FDCALG procedure.

MFM



Timebase 1 usec/div
Vertical 2 v/div
Invert B and add to A
Minimize the glitches.

Signal "RDA" is used as a trigger at Pin 9 of One-Shot U25. This one-shot is used to generate the Raw Data pulse for the FDC chip. See "RAW DATA".

"RDA" is also used at U28, which is part of the Clock Recovery circuit.

RAW DATA — From Pin 12 of U25. Pin 12 will produce a negative-going 200 nanosecond pulse with every data input transition.

The "RAW DATA" signal is routed to Pin 27 of FDC U6. The serial data stream appearing at this input will be latched (through the RCLK window) into the data Shift Register of the FDC. The FDC will execute signal "DRQ" (see same) when this Register is loaded.

2 MHZ (TP 26) — From Pin 6 of VCO U27. This is the nominal 2 MHz RCLK frequency before it is divided by the two parts of U29, and the one part of U14. Pin 5 of U14 will output two different RCLK signals: 500 KHz for the MFM mode, and 250 KHz for the FM mode. These signals are used as the Recovery Clock for the FDC through U4 and U7. See signal FM/MFM* for supporting information.

The Clock Recovery Circuits.

TP 26: The frequency of the square-wave signal appearing at this test point is controlled by the DC voltage at TP 25.

A voltage of 3.5 volts at TP 25 will set the nominal frequency of the VCO at TP 26 to 2 MHz.

Note: The 3.5 volts mentioned above is only an average. Do not use this voltage to set the VCO frequency. Follow the adjustment outlined in the FDCALG procedure.

TP 25: The voltage at this test point is used to set the frequency of the VCO. See TP 26. This voltage will vary from a low of about 1.6 volts, to a high of about 5 volts. The setting of Potentiometer R32 will determine the exact voltage. Diodes CR3 and CR4 are used to set the voltage limits at TP 25 to a low of -6ØØ millivolts, and a high of +5.6 volts.

The voltage at TP 25 will always be lower than the voltage at Pin 6 of U26 by a factor of Ø.45. This reduction factor is set by the resistance values of R34 and R35.

TP 5: Regulated +5 volts. This voltage is used as a supply source for VCO U27. It is also used to set the absolute upper voltage limit at TP 25 to +5.6 volts.

During initialization (power on), Capacitor C25 will charge through Diode CR2 to the +5.6 volt source of Zener, CR1. The 6ØØ millivolt barrier potential of CR2 will limit the charge of C25 to +5 volts.

U26: In the "Insert Diskette" mode, the voltages at Test Points 27 and 28 should be at the logic zero level. In this state, the output voltage appearing at Pin 6 of U26 should be at about +8 volts (this assumes that the previous alignment on the FDC card was done correctly, and that the setting of R32 hasn't been touched. See TP 25 and TP 26). This voltage is an offset, produced by the current through Transistor Q1, and sensed at the input of U26.

If the voltage at Pin 6 of U26 appears abnormal, or does not vary when Potentiometer R32 is adjusted, check the voltage at the wiper of this potentiometer first. This voltage should vary from approximately -6.6 volts to -1Ø volts as the wiper is varied from one extreme to another. If the voltage does not change, check the potentiometer for bad connections. Also check Transistor Q1 to see if it is open.

If the potentiometer and transistor check good, then the operational amplifier should be checked next. Give this device a GOOD-BAD check by disconnecting the collector lead of Transistor Q1 from the circuit. With the transistor electrically out, the voltage at Pin 6 of U26 should be at zero volts, +/- 2ØØ millivolts (for this output indication to be true, TP 27 and TP 28 must both be at a logic low: check this to be sure). The operational amplifier should be considered bad if the voltage at this Pin is anything other than zero volts. Note: the output of a bad operational amplifier will usually latch to the plus or minus supply (+/- 12 volts).

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Glossary - Sheet 2

Only the mnemonics originating from Sheet 2 of the Early FDC schematic will be covered under this heading.

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CLOCK — From Pin 44 of the Model II System Bus. This is the 4 MHz System Clock. It is buffered at Pin 2 of U34 to become signal "CLOCKI" (see same).

Note: U34 is an open collector device. It will open, or switch to a high Z state with a logic high. Resistor R51 (located on the left side of U22 on the schematic) is used to pull-up the line to +5 volts.

CLOCKI — From Pin 2 of Buffer U34. This 4 MHz signal is applied to Pin 25 of PIO U22. The PIO will use this clock to synchronize certain internal signals.

"CLOCKI" is also used at Pin 11 of U14 where it is divided by 2 to emerge at Pin 9 as a 2 MHz signal. This 2 MHz signal is tied to Terminal "A", which is jumpered to Terminal "B", then further to Pin 24 of FDC U6.

B/A* — To Pin 6 of PIO U22. From Address line AØI. This is the PIO "B" Port or "A" Port Select signal. The logic status of this signal will define which Port will be accessed during a data transfer between the PIO and CPU. A logic low at this input will select the "A" Port of the PIO. This selection is an indication that the CPU is in the process of reading Port EØ to check the FDC and Printer Status signals.

The "B" Port of the PIO will be selected when Pin 6 is at a logic high. This selection is an indication that the CPU is in the process of writing to Port E1 of the PIO. The CPU will load the "B" Output Register with ASCII data for the printer during this write.

C/D* To Pin 5 of PIO U22. From Address line AlI.

This is the PIO Control or Data Select signal. A logic high on this Pin during a CPU write to Port E2 will be interpreted by the PIO as a control, or command signal used for the configuring of the "A" Port. The "B" Port of the PIO will be "commanded", or configured when the CPU is writing to Port E3.

When this signal is a at a logic low at Pin 5, the PIO will decode this logic status as a Data Select signal, and that the CPU is in the process of transfering data between the CPU and the "A" or "B" Ports of the PIO. The transfer Port will depend on the logic status of signal "B/A*" (see same).

TWOSIDED From Pin 1Ø of the Drive Bus (label it!). The inverted result is tied to Pin 14 of PIO U22.

"TWOSIDED" is an optional signal that is available from a double sided diskette. A second Index LED sensor is used by the drive to detect when a double sided diskette is installed.

The Two Sided signal will be at a logic low at Pin 1Ø of the Drive Bus when a double sided diskette is in use.

DISKCHANGE From Pin 12 of the Drive Bus (label it!). The inverted result is tied to Pin 13 of PIO U22.

This signal will become asserted, or switch to a logic low at Pin 12 of the Drive Bus when the diskette is changed or when the drive door lever lock is open.

The exact logic used to generate this signal will depend on the type of drive that is in use.

PRIME From Pin 12 of PIO U22. This is an optional Software Reset signal to the printer, and is functionally identical to a Power On Reset. This signal is not in use at this time.

FAULT — To Pin 11 of U9, where it is inverted to Pin 1Ø of PIO U22. This is the Fault Detect signal from the printer. The exact fault conditions that will cause this signal to be present will depend on the type of printer. As an example, the DW II printer will assert this signal whenever an error is detected in the Select or Space servo circuits, or when the printer runs out of ribbon.

An asserted "FAULT" signal will appear as a logic low at Pin 1Ø of the PIO. The System will not attempt to load data to the printer when this signal is asserted.

Note: When no printer is interfaced to the System, Resistor R12 will keep the line at Pin 11 of U9 in the Fault state for the reason mentioned above.

PSEL — To Pin 9 of PIO U22. "PSEL" is an optional signal from the printer. Its logic status is usually controlled by the ON LINE/OFF LINE switch located on the printer's console.

An ON LINE condition will place a logic low at Pin 9 of the PIO.

PE — To Pin 8 of the PIO U22. This is the optional Paper Empty signal from the printer.

A paper empty condition will place a logic high at Pin 8 of the PIO.

BUSY — To Pin 5 of U15, inverted to Pin 7 of PIO U22. This signal will be asserted at a logic high when the printer is not ready. The conditions which will cause the printer to assert this signal will depend on the type of printer. Some of the conditions that could generate this signal are listed on the next page.

* Data Buffer Full.

* Reset State.

* OFF LINE Mode.

* Printer Circuits In Error.

* Out Of Ribbon.

* Printer Cover Open.

Note: Resistor R5 will keep the line at Pin 5 of U15 in the Busy state. This condition will prevent the System from trying to load the printer Port with data.

PACK* (TP 16)

From Pin 19 of the printer connector.

Signal "PACK*" is a 5 to 1Ø microsecond negative-going pulse from the printer. An asserted "PACK*" signal is an indication that the previous byte of data from the PIO has been loaded into the Buffer of the printer. This signal is also used to inform the PIO that the printer is ready for another data byte transfer.

The "PACK*" signal is applied to Pin 17 of the PIO. Pin 17 is the B Strobe input of the PIO.

PSTB* (TP 22)

From Pin 4 of One-Shot U37. To Pin 1 of the printer connector.

Signal "PSTB*" will be generated a few nanoseconds after the valid ASCII data to the printer appears at the "B" Port of the PIO. This 1.5 microsecond negative-going pulse is used to latch in the ASCII data byte into the Buffer of the printer.

"PSTB*" originates from Pin 21 of the PIO. This is the B Ready output of the PIO. The B Ready signal is normally at a logic low and will switch to a logic high only when the "B" Port Output Register is loaded with an ASCII byte of data from the CPU. One-Shot U37 will generate signal "PSTB*" when Pin 21 of the PIO switches to a logic high. Note: Pin 3 of U37 should show an inversion bubble. Draw it in.

IORQI* To Pin 36 of PIO U22. From Pin 16 of Buffer U36/1 where it is called "IOCYCI*" (see same).

INTRQI* From Pin 23 of PIO U22. To Pin 13 of U34 where it is buffered at Pin 12 to become signal "INTRQ*". Signal "INTRQ*" is applied to Pin 11 of the Model II System Bus where it will travel back to Pin 11 of the CPU Board and end up at the "INT*" input of the CPU.

Signal "INTRQI*" is the Interrupt Request signal from the PIO. The conditions which will execute this signal will depend on how the PIO is programmed to service interrupts. Refer to signal "INTRQ" on page 2-19 for supporting information.

Early FDC Board Test Points

TP 1	Not listed
TP 2	Not listed
TP 3	Not listed
TP 4	TRKØ*.....Pin 34 of U6/1
TP 5	+5 volts....Cathode of CR2/1
TP 6	Not listed
TP 7	Not listed
TP 8	Not listed
TP 9	READ DATA...Pin 6 of U13/1
TP 1Ø	CWD.....Pin 4 of U16/1
TP 11	RDY.....J1, Pin 22

TP 12 STEP*.....Pin 2 of U4/1

TP 13 INTRQ (FDC).Pin 39 of U6/1

TP 14 CEFDC*.....Pin 6 of U8/1

TP 15 XFERRQI*....Pin 38 of U6/1

TP 16 PACK*.....Pin 17 of U22/2

TP 17 8 MHZ.....Pin 9 of U36/1

TP 18 CEPIO*.....Pin 8 of U8/1

TP 19 CLK (2 MHZ).Pin 24 of U6/1

TP 2Ø RCLK x2.....Pin 8 of U3Ø/1

The frequency at this test point will depend on the density mode of operation:

MFM: 1 MHz

FM: 5ØØ KHz

TP 21 HLD*.....Pin 1Ø of U4

TP 22 STROBE*.....Pin 4 of U37

TP 23 RCLK.....Pin 26 of U6/1

TP 24 RDA.....Pin 13 of U25/1

TP 25 A DC voltage which is limited to a range from -6ØØ millivolts to +5.6 volts. This voltage is is used to set the VCO frequency. Follow the alignment outlined in the FDCALG procedure.

TP 26 VCO 2 MHz...Pin 6 of U27/1.

TP 27 SPEEDUP.....Pin 5 of U28/1.

The signal at this test point should be at a logic low with no drive activity.

TP 28 SPEEDDOWN...Pin 9 of U28/1.

The signal at this test point should be at a logic low with no drive activity.

TP 29 CLOCKI.....Pin 2 of U34/2.

TP 3Ø This is the stretched (2.5 microseconds) positive-going LATE signal used for Write Precompensation.

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Early FDC Board Jumper Configuration

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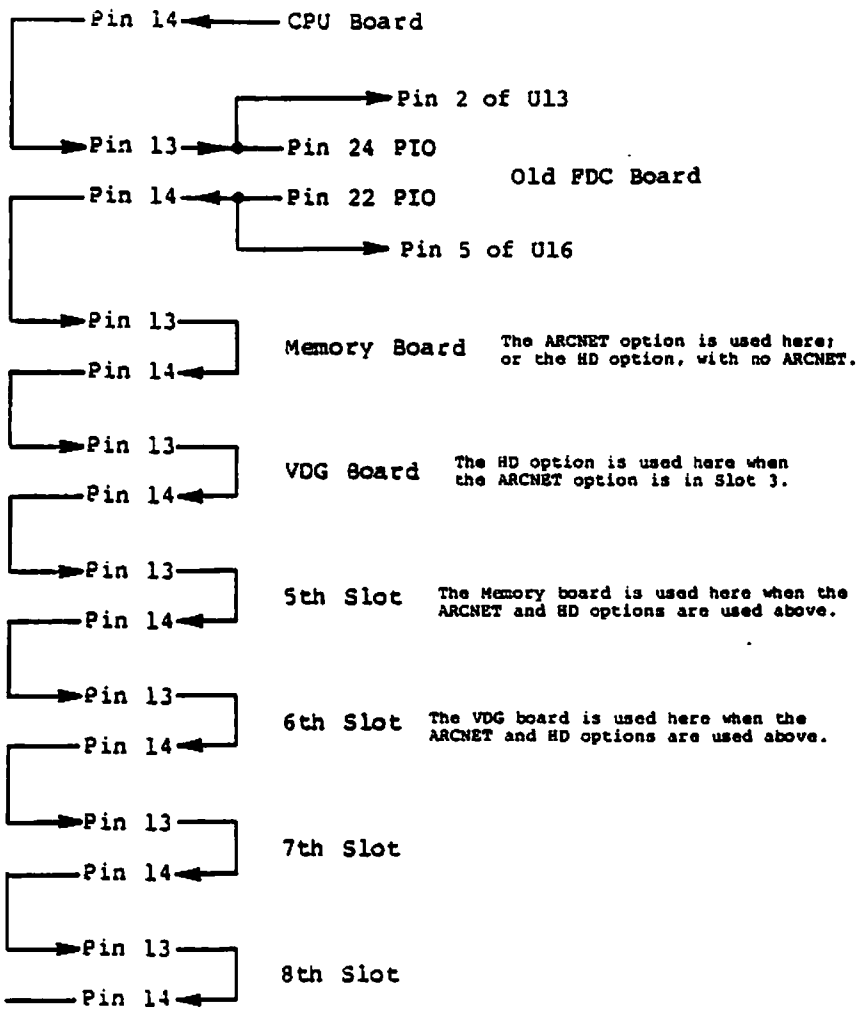
A to B	2 MHz Option.
3 to 4	TG43 Enable.
6 to 7	25Ø nanosecond shift for Write Precompensation.

Mother Board Interrupt Loop



Note: All boards with devices tied to the interrupt loop must occupy slots adjacent to each other. This must be done to keep the interrupt chain intact. The farthest board from the CPU board will have the lowest interrupt priority.

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Section Three

Model II FDC Board - Late

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Contents

The listings in this glossary are divided into 2 sections, respective to the 2 sheets of the FDC schematic.

When a signal from one sheet is referenced to another, a pointer, "/#", will be used to indicate the sheet: i.e. From Pin 6 of U29/2 To Pin 26 of U11/1.

The latest revised FDC Board is REV B. The schematics contained in the manual reflect the circuits which are on the REV Blank Board. The circuit changes between the FDC revisions of this series are minor.

Index for Late FDC Board Signals

Glossary - Sheet 2

Only the mnemonics originating from Sheet 2 of the Revised FDC schematic will be covered under this heading.

XF* From Pin 6 of U21.

Note: Pin 6 of U21 isn't labeled on the schematic. See below.

"XF*" decodes the low-order address nibble as FH to access Port EF. It is applied to Pin 4 of U22 where it is NANDed with signal "EX*" at Pin 5 (see same).

EX* From Pin 8 of U21. This signal decodes the upper address nibble as EH to access Ports EØ through EF. The Ports allocated to the FDC Board are summarized below.

PORT #	ALLOCATION	FUNCTION
E0H	PIO Port A – Data	Printer and FDC INT. status
E1H	PIO Port B – Data	Printer Data (output)
E2H	PIO Port A – Control	Configuring Port A
E3H	PIO Port B – Control	Configuring Port B
E4H	FDC Status/CMD Register	FDC Status and CMD
E5H	FDC Track Register	Current Track Add.
E6H	FDC Sector Register	Current Sector Add.
E7H	FDC Data Register	Data To or From Diskette
E8H	Soft FDC Reset	Out Resets FDC
EFH	Drive Select Latch	Drive, Mode, Side Select

Signal "EX*" is applied to Pin 5 of U22 where it is NANDed with signal "XF*" (see same) to become signal "DRSEL*" (see same) at Pin 8 of U22.

Signal "EX*" is also applied to pins 2 and 13 of U22 to enable the gates for Address lines "A3I" and "A2I". These address signals, along with address signals "A1I" and "AØI", are used as inputs to BCD-To-Decimal Decoder U23.

Note: Address line "A2I" at Pin 1 of U22 is incorrectly labeled on the schematic as "A21*". Address line "A3I" is incorrectly labeled at Pin 12 of U22 as "A31".

DRSEL* (TP 2Ø) From Pin 8 of U22. This is the Drive Select signal, which will be asserted when the CPU is in the process of writing to Port EF.

This signal is applied to Pin 9 of U11/1 where it is labeled as "DRVSEL*". Signal "DRVSEL*" is incorrectly labeled on the schematic as "DRUSEL*".

Signal "DRVSEL*" is used to latch-in the following:

* The BCD bit code to BCD-To-Decimal Decoder U36. This code will cause one of the output lines of the decoder to go to a logic low to select one of two possible internal drives ("DSØI*" or "DS1I*"), or one of three possible external drives ("DS1E*", "DS2E*", or "DS3E*"). Note: Drive select signal "DS1E*" is incorrectly labeled at Pin 4 of U1Ø as "DS1E8". Also, the inversion bubbles at pins 2, 3, 5, and 1Ø of U36 are not shown on the schematic: draw them in. Label Pin 2 of U36 "TP 1".

  How Drive Ø is selected is given as an example below.

  A logic low at Pin 2 of U36 will select Drive Ø when the BCD input has Pin 15 at a logic high, and pins 14, 13, and 12 are at a logic low.

* Data Bit 6. The logic status of this bit is used to produce the Side Select signal. Side Ø of the drive will be selected when this bit is at a logic high at Pin 12 of U11/1.

* Data Bit 7. The logic status of this bit is used to produce the Double Density Enable signal. A logic high at Pin 15 of U11/1 will place the FDC in the Double Density mode. See signal "DDEN*".

CEPIO* (TP 11) — From Pin 1 through 4 of BCD-To-Decimal Decoder U23. To Pin 4 of PIO U12/1. This is the Chip Enable signal for the PIO.

The PIO chip will be selected when this signal is at a logic low. This selection will allow the CPU to communicate with the PIO. Communication with this chip will be in progress when the CPU is addressing Ports EØ through E3. The functional allocation of each of these Ports is listed on page 3-3.

Signal "CEPIO*" is also used at Pin 9 of U1 of the Bus Steering Logic. The purpose of this circuit is to control the logic level of signal "CPUIN" (see same) when the CPU is in the process of reading a Port Address of the PIO. Note: This portion of U1 is incorrectly drawn with an OR gate symbol. Change this symbol to a NAND gate.

CEFDC* (TP 8) — From pins 5, 6, 7, and 9 of BCD-To-Decimal Decoder, U23. To Pin 3 of FDC U18. This is the Chip Enable signal for the FDC.

The FDC chip will be selected when this signal is at a logic low. This selection will allow the CPU to communicate with the FDC. Communication with this chip will be in progress when the CPU is addressing Ports E4 through E7. The functional allocation of each of these Ports is listed on page 3-3.

Signal "CEFDC*" is also used at Pin 2 of U13/1 where it is ANDed with signal "IN*" to produce a logic high at TP 14. This logic high signal is used to enable the Drivers of Buffers U19/1 and U2Ø/1. The Receivers of these Buffers will also be disabled at this same time.

Note: Buffers U19 and U2Ø are electrically wired between the Internal Data Bus of the FDC Board and the Data Access Lines of the FDC chip. These Buffers are used to reverse the logic levels of the data going to, and coming from the FDC chip. This correction is necessary because the FDC chip uses an inverted internal bi-directional bus to transfer all Data, Control, and Status information.

"CEFDC*" is also used at Pin 1Ø of U1 of the Bus Steering Logic. The purpose of this circuit is to control the logic level of signal "CPUIN" (see same) when the CPU is in the process of reading a Port Address of the FDC. Note: this portion of U1 is incorrectly drawn with an OR gate symbol. Change this symbol to a NAND gate.

E8* — From Pin 1Ø of BCD-To-Decimal Decoder U23. To Pin 1 of U34 where it is NANDed with signal "OUT*" (see same), then further, to produce signal "SOFTMR*" (see same).

Note: Although this redesigned FDC Board is fully compatible with the old design, an additional Port has been provided to function as a Software Master Reset to the FDC Board. This feature allows the programmer to reset the FDC Board and recover a hang-up condition should it ever happen, even though this condition will rarely occur with this new FDC chip set.

SOFTMR* (TP 7) — From Pin 11 of U14. This is the Software Master Reset signal. This signal can be activated by a Master System Reset with signal "RESETI*" at Pin 12 of U14, or by a programmed reset with signal "E8*" at Pin 13 of U14. See signal "E8*".

To Pin 19 of FDC U18. A logic low on this input pin will reset the FDC chip and load an Ø3H (RESTORE command) into the Command Register. The Not Ready Bit (Bit 7) in the Status Register will also reset during this time. The RESTORE command will be executed when the reset signal is brought to a logic high. This RESTORE will happen regardless of the state of the Ready signal from the drive.

Signal "SOFTMR*" is also applied to Pin 2 of U14, then further on to Pin 19 of the Write Precompensation and Clock Recovery chip U28. Pin 19 of this chip is the fourth phase of the 4-Phase input used to generate the desired Write Precompensation delay. The first three phases tie directly to the output lines of the Four Phase Clock Generator U29. The fourth phase out of U29 is looped through U14 before ending up at Pin 19 of U28. A low at Pin 19 is used to reset the Strobe line of U28 in anticipation of the next Data Write pulse.

OUT*
(TP 15)

From Pin 6 of U34. This signal is the logical product of signals "WRI*" and "IORQ*".

Signal "OUT*" will be asserted when the CPU is in the process of writing to any Port.

This signal is applied to Pin 1Ø of U22 to gate the Port EF signal through to Pin 8 of U22, where it becomes signal "DRSEL*" (see same).

Signal "OUT*" is used at Pin 2 of FDC U18. This is the Write Enable signal to the chip. A logic low at this input pin will cause the FDC to gate in the data on the Data Access Lines into the selected Register when the Chip Select signal at Pin 3 is at a logic low.

"OUT*" is also applied to Pin 2 of U34 to gate the Port E8* signal through to Pin 11 of U14. This signal is labeled "SOFTMR*" (see same) at Pin 11.

IN*
(TP 31)

From Pin 8 of U34. This signal is the logical product of signals "RDI*" and "IORQ*".

Signal "IN*" will be asserted when the CPU is in the process of reading any Port. This signal is used at Pin 4 of FDC U18. This is the Read Enable signal to the chip. A logic low at this input Pin will cause the FDC to gate out the data on the Data Access Lines from a selected Register when the Chip Select signal at Pin 3 is at a logic low.

Signal "IN*" is used at Pin 1 of U13/1, where it is used to control the direction of Buffers U19 and U2Ø. See signal "CEFDC*".

"IN*" is also applied to Pin 13 of U13 of the Bus Steering Logic. This signal is used to gate through signals "CEFDC*" (see same) and "CEPIO*" (see same) when the CPU is in the process of reading any of the FDC or PIO Ports. See signal "CPUIN".

CPUIN
(TP 23)

From Pin 1Ø of Inverter U2. Note: This Pin is incorrectly labeled Pin 12: change it to Pin 1Ø. "CPUIN" is the logical (TP 23) output of the Bus Steering Logic. This signal is used at pins 1 and 15 of Buffers U3Ø and U31 to enable the Bus Drivers when one of the conditions outlined on the next page occurs.

* When the CPU is in the process of reading a Port Address of the PIO.

  Under this condition, signal "CEPIO*" will be asserted at Pin 9 of U1. This indicates that the CPU is in the process of accessing any one of the four PIO Ports. If this Port access is a Read, then signal "IN*" at Pin 13 of U13 will also be at a logic low. The result of these two signals being asserted at the same time will cause pin 11 of U13 to go low. This negative-going signal will trigger the rest of the logic to produce signal "CPUIN".

* When the CPU is in the process of reading a Port Address of the FDC.

  Under this condition, signal "CEFDC*" will be asserted at Pin 10 of U1. This indicates that the CPU is in the process of accessing any one of the four FDC Ports. If this Port access is a Read, then signal "IN*" at Pin 13 of U13 will also be at a logic low. The result of these two signals being asserted at the same time will cause pin 11 of U13 to go low. This negative-going signal will trigger the rest of the logic to produce signal "CPUIN".

* When the CPU is in the process of acknowledging an Interrupt Request from the PIO.

  Under this condition, signal "INTAK*" will appear as a logic low at Pin 5 of U14. This indicates that the CPU is in the process of granting an Interrupt Acknowledge to the PIO. This negative-going signal at Pin 5 will trigger the logic to produce signal "CPUIN". See signal "INTAK*".

INTAK* From Pin 12 of U5. This signal will be asserted when the CPU is in the process of granting an Interrupt Acknowledge to the PIO.

"INTAK*" is a conditional signal. The three conditions listed on the next page must be met before this signal can be generated.

Conditon 1: Pin 13 of U5 must be at a logic high.

This condition will be met when signal "IEOUT" from Pin 22 of the PIO is at a logic low. This low is an indication that the PIO has generated an Interrupt Request. This signal will remain low until the Interrupt is acknowledged by the CPU. Signal "IEOUT" is also applied to Pin 14 of the Model II System Bus.

The low level "IEOUT" signal is inverted at Pin 2 of U2 to place a logic high at Pin 13 of U5, thus meeting the first condition.

Condition 2: Pin 2 of U5 must be at a logic high.

This second condition will be true when signal "IEIN" is at a logic high at Pin 2 of U5.

Note: "IEIN" and "IEOUT" are signals of the Z8Ø interrupt structure. This structure allows up to four Z8Ø family devices to be connected in a daisy chain fashion without any additional logic. In the Model II, a 4 Bit Adder device (U23 on Sheet 2 of the CPU schematic) has been added to the chain to improve the propagational characteristics of the daisy chain signal bus. This improvement in propagation time allows the System to add up to four more devices of the same family to the interrupt chain when the need arises.

The basic Model II has only four devices tied to the interrupt structure. Three of these are on the CPU Board, while the fourth is on the FDC Board. The interrupt priority is as follows: From CTC (highest priority), to SIO, to DMA, to PIO (lowest priority).

Since the inception of the Model II, optional Boards have become available which contain devices that are tied to the interrupt structure, specifically, the ARCNET and HD Boards. Both of these Boards have CTC devices which are tied into the daisy chain interrupt loop. The interrupt priority of these Boards follow the PIO device on the FDC Board, namely:

From PIO (highest priority), to ARCNET, to HD (lowest priority).

Note: The interrupt levels for external Boards is set by the order of the Boards. There must be no empty slots.

Back to Condition 2.

Signal "IEIN" originates from Pin 13 of the Model II System Bus. This line feeds back to Pin 14 of the same Bus to the CPU Board. This signal is called "IEOUT" on the CPU schematic, because it is the IEOUT signal of the lowest priority device on the CPU Board. A diagram of the Model II daisy chain interrupt loop is illustrated on page 3-37.

"IEIN" will be at a logic low at Pin 2 of U5 when any one of the three devices on the CPU Board is in the process of generating an interrupt Request. When no device on the CPU Board is requesting an Interrupt, Pin 2 will be at a logic high. This high meets the second condition.

Condition 3: Pin 1 of U5 must a logic high.

This condition will be met when the CPU is in the process of granting an Interrupt Acknowledge to any Z8Ø device linked to the Systems priority interrupt structure.

During the Interrupt Acknowledge sequence, signal "IORQI*" at Pin 3 of U33 will be low, along with signal "SYNCI*" at Pin 11 of U33. Tracing these signals from U33 will show that a high will appear at Pin 1 of U5. This high at Pin 1 meets the final condition needed to generate signal "INTAK*".

Note: As you are already aware, the Z8Ø CPU employs both types of interrupts: maskable (INT* Input) and non-maskable (NMI* Input). The CPU will service these interrupts in a specific sequence. Both of the interrupt inputs will be sampled on the rising edge of the sys-

tem clock in the last T state of the last instruction cycle. However, if the "BUSRQ*" input of the CPU is asserted at the same time, it will be processed before any other Interrupts. As for the daisy chain interrupts, the CPU will always service the higher priority devices first.

Getting back to U5. With pins 2 and 13 at a logic high, signal "INTAK*" will be generated as soon as Pin 1 of U5 goes to a logic high. The high at Pin 1 is an indication that the CPU has begun to service the PIO's Interrupt Request.

As a further note, should a device on the CPU Board output an Interrupt Request before the PIO's request is serviced, Pin 2 of U5 will switch to a logic low and prevent signal "INTAK*" from being generated. This same logic low will also appear at Pin 24 of the PIO. This low at the PIO will keep it in the "interrupt pending" state until the CPU has completed servicing the Interrupt of the higher priority device. When this service is completed, signal "IEIN" at Pin 24 of the PIO and pin 2 of U5 will switch back to a logic high, and the CPU will return with another Interrupt Acknowledge to service the Interrupt Request of the PIO.

The daisy chain signals will return to their quiescent states when the servicing process is complete.

IEIN — From Pin 13 of the Model II System Bus. To Pin 2 of U5 and Pin 24 of the PIO. For a functional understanding of this signal refer to signal "INTAK*", and also to the diagram on Page 3-37.

IEOUT — From Pin 14 of the Model II System Bus. To Pin 9 of U2 and Pin 22 of the PIO. For a functional understanding of this signal refer to signal "INTAK*", and also to the diagram on Page 3-37.

TG43 — From Pin 29 of FDC U18. This signal will be asserted between Tracks 44 through 76 in the Double Density mode.

Signal "TG43" is used at Pin 9 of U28 to enable the Write Precompensation circuit of this chip in the Double Density mode.

This signal is also applied to Pin 2 of Buffer U9, then further, where it is inverted at pins 12 and 1Ø of U7 to become signals "LOCURI*" and "LOCURE*", respectively. These are the Low Current signals which are connected to Pin 2 of the Internal and External Drive Buses. In the Double Density mode, "TG43" is used to reduce the Write Current of the drive by 25% when the head is positioned between tracks 44 through 76.

The typical peak-to-peak Write Current for an 8-inch drive before Track 44 is approximately 1Ø milliamperes.

WG — From Pin 3Ø of the FDC U18. This signal is set to a logic high before a Write is performed to the diskette.

Signal "WG" is used at Pin 7 of U28 to disable the data recovery circuits of this chip.

"WG" is also applied to Pin 14 of Buffer U9, then further, where it is inverted at pins 2 and 4 of U8 to become signals "WGI*" and "WGE*", respectively. These are the Write Gate signals which are connected to Pin 4Ø of the Internal and External Drive Buses.

The Write Gate signal is used to enable the write circuit of the drive before an actual Write is performed to the diskette.

FDCINT (TP 12) — From Pin 39 of FDC U18. This is the Interrupt Request signal of the FDC chip: it is normally kept at a logic low. It will be pulled to a logic high by Resistor R15 at the completion of any command, and will be pulled back to a logic low after the Status Register is read or the Command Register is written to.

Signal "FDCINT" is applied to Pin 15 of PIO U12/1. Pin 15 is Bit Ø of the "A" Port of the PIO. The PIO is programmed to monitor the logic status of this bit. The PIO will generate an Interrupt Request to

the CPU when the Status of this bit is a logic high. The CPU will then service this Interrupt (under the conditions outlined by signal "INTAK*") by performing a Read operation to Port EØ. The Status of all of the input lines of the PIO's "A" Port will be checked during this read. During this Read operation, the logic high of Data Bit Ø will inform the CPU that the FDC chip has generated an Interrupt Request.

Upon completion of this Read to Port EØ, the CPU will perform another Read operation, but this time to Port E4 to check the bit levels of the FDC's Status Register. The meaning of the Status Bits in this Register will be a function of the type of command previously executed by the FDC. After reading Port E4, the CPU will most likely do a Write operation to this same Port to load the Command Register of the FDC with the next command instruction.

DRQ (TP 22)

From Pin 38 of FDC U18. This is the Data Request signal from the FDC. Note: this signal is incorrectly labeled on the chip as "DKQ". Change it to "DRQ". This signal is normally kept at a logic low. It will be pulled to a logic high by Resistor R28 when the FDC Data Register contains assembled data during a Read operation, or when the FDC Data Register is empty during a Write operation. This signal is pulled back to a logic low after the DMA services the FDC by reading or loading the Data Register.

This signal is applied to Pin 5 of U27/1, where it is buffered at Pin 6 of U27/1 to become signal "XFERRQ" (Note: Terminal L is normally jumpered to Terminal M). Signal "XFERRQ" is then routed to Pin 41 of the Model II System Bus where it will travel back on the same Bus to Pin 41 of the CPU Board. "XFERRQ" is applied directly to Pin 25 of the DMA chip on the CPU Board. Pin 25 is the Ready input to the DMA.

Note: Most of the data transfers from Drive-to-Memory, or Memory-to-Drive are handled by the DMA. The DMA is used because its data transfer speed is much faster then the CPU.

The DMA can be programmed to operate in any of three modes: Byte, Burst or Continuous. The Byte mode is used for all data transfers in the

Model II. In this mode, the DMA and CPU will alternately share the System Bus during data transfer operations. This time sharing of the System Bus during this period is called "interleaving". This interleaving allows the CPU to continue with its monitoring functions of the System.

Back to signal "XFERRQ". This input signal is continuously monitored by the DMA to determine when the drive is ready for a Read or Write operation. When this signal is asserted, the DMA will ask the CPU for control of the System Bus by generating signal "BUSRQ*". Signal "BUSAK*" is used to inform the DMA that the CPU has relinquished control of the System Bus.

DIR (TP 6) — From Pin 16 of FDC U18. This is the Head Direction signal for the drive logic. This signal works in conjunction with signal "STEP" (see same). When signal "DIR" is a logic high, the head direction will be inward, or towards Track 76 when it is stepped by signal "STEP". The converse will be true when this signal is at a logic low. In this low state the head will step outward, or towards Track Ø. As a special note, the Direction signal will appear approximately 12 microseconds before the first Step pulse is generated.

Signal "DIR" is applied to Pin 4 of Buffer U9, then further, where it is inverted at pins 6 and 8 of U8 to become signals "DIRI*" and "DIRE*", respectively. These signals are tied to Pin 34 of the Internal and External Drive Buses.

STEP (TP 9) — From Pin 15 of FDC U18. This is a 2 microsecond positive-going pulse used to move, or position the drive head over the diskette media. For every Step pulse that is issued by the FDC chip, the drive head will move one track location in a direction determined by the logic status of signal "DIR" (see same). The first Step pulse will appear approximately 12 microseconds after the "DIR" signal is generated.

Signal "STEP" is applied to Pin 12 of Buffer U9, then further, where it is inverted at pins 1Ø and 12 of U8 to become signals "STEPI*" and "STEPE*", respectively. These signals are tied to Pin 36 of the Internal and External Drive Buses.

HLD*
(TP 28)

From Pin 6 of U2. This signal is the inverted result of signal "HLD" at Pin 28 of FDC U18.

Signal "HLD*" is used to control the loading of the drive head against the diskette media. The drive head is loaded when this signal is asserted at a logic low.

The "HLD*" signal is buffered at U27 to become signals "HLDI*" and "HLDE*" at pins 2 and 4, respectively. These signals are tied to Pin 18 of the Internal and External Drive Buses.

The negative-going edge of signal "HLD*" is also used as a trigger at Pin 9 of One-Shot U15. This one-shot is used to keep signal "HLT" (see same) negated for a period of approximately 5Ø milliseconds.

Signal "HLD*" is also applied to Pin 1 of U3/1, which is part of the Raw Data Read Enable logic. Refer to signal "RDATA*" to see how this logic is enabled.

HLT
(TP 4)

To Pin 23 of FDC U18. This is the Head Load Timing signal to the FDC chip. The FDC chip will assume that the drive head is loaded, or engaged when this input signal switches to a logic high.

The initialization of this signal will be delayed with respect to the negative-going edge of signal "HLD*" by approximately 5Ø milliseconds. One-Shot U15 will produce this delay whenever it is triggered by "HLD*". See signal "HLD*". This delay is necessary to allow the drive head to settle, or engage completely before the FDC does an actual Read or Write operation to or from the diskette media.

Note: The Head Load Timing is a drive specification. The head engagement time for most drives will fall between the range of 3Ø to 1ØØ milliseconds. U15 is used to set the HLT to an average of approximately 5Ø milliseconds.

Signal "HLT" is also applied to Pin 9 of NAND gate U5, which is part of the Raw Data Read Enable logic. Refer to signal "RDATA*" to see how this logic is enabled.

Note: The FDC will be able to read from or write to the diskette media only when signals "HLT" and "HLD" are both true at pins 23 and 28 of the FDC chip.

Pin 1 of FDC U18.

This Pin is incorrectly labeled as "WDIN". According to the FD179X spec sheet, this Pin is internally connected to a back bias generator and must be left open. However, in the early days of the Model II, it was found that the FDC chip could become thermal. This thermal problem was causing Read / Write errors, erratic operation, and miscellaneous other failures of the disk I/O. A fix was made to eliminate these problems by connecting Pin 1 of the chip to ground through a 2.7 volt Zener.

As a further note, when disk I/O problems are being encountered, don't hesitate to hook a scope probe to Pin 1 of the FDC chip. What you see there could tell you a lot about the chip. Make sure that the DC level at this Pin is at minus 2.7 volts. Also, this voltage level should be clean, free of RF noise, or spikes. Don't guesstimate, just replace the FDC chip if it appears noisy.

MR* — To Pin 19 of FDC U18. This is the Master Reset input to the FDC chip. This input is controlled by signal "SOFTMR*" (see same).

A logic low on this input Pin will reset the FDC chip. A RESTORE (Ø3H) will be loaded into the Command Register, and the Not Ready Status Bit will be reset during this time. When this input returns to a logic high, the RESTORE command will automatically be executed, regardless of the logic state of signal "READY" (see same) at Pin 32.

RDD* (TP 29) — To Pin 27 of FDC U18. This is the Raw Read Data input to the chip. This is the data input signal from the drive. The input will appear as a negative-going 25Ø nanosecond pulse for each recorded flux transition. This input line is labeled "RDATA*" (see same), and it originates from Pin 12 of One-Shot, U6/1.

CLK (TP 18) — To Pin 24 of FDC U18. This is the Master Clock input to the FDC chip which is used for internal timing references. The frequency of this Clock will be 2 MHz for 8-inch drives, and 1 MHz for 5-inch drives. The input line is labeled "FDCLK" (see same), and it originates from Pin 9 of Divider U26/1.

READY (TP 3)

To Pin 32 of FDC U18. This input to the FDC chip is used to indicate the readiness of the disk drive. This signal must be at a logic high before any Read or Write commands can be issued. There are some exceptions: see signal "MR*", also, the spec sheet on the FD179X.

The exact variables involved to produce this signal will depend on the type of drive in use. A few of the things a drive could check before producing this signal are listed below.

* Check if the drive is selected.
* Check that the drive door is closed.
* Check to see if the drive spindle is up to speed.
* Check the Read/Write logic to determine if the drive is in readiness for a Read or Write operation.

Signal "READY" is the inverted result of the signal appearing at Pin 4 of Multiplexer U17. The "READY" signal can be sourced from the drive logic of any internal or external drive by signal "READYI" or "READYE" which are tied to Pin 22 of the Drive Bus. The logic status of signal "INT*/EXT" (see same) at Pin 1 of U17 will determine the input selection.

WPRI* (TP 19)

To Pin 36 of FDC U18. This input signal is used by chip to detect if the diskette is write protected. This input will be sampled whenever a Write Command is received. A logic low at this input will terminate the command and set the Write Protect Status Bit.

This signal comes from Pin 7 of Multiplexer U17. It can be sourced from the drive logic of any internal or external drive by signal "WPRTI" or "WPRTE" which are tied to Pin 44 of the Drive Bus. The logic status of signal "INT*/EXT" (see same) at Pin 1 of U17 will determine the input selection.

IP*
(TP 13)

To Pin 35 of FDC U18. This is the Index Sector input pulse from the drive. It is used to inform the FDC chip when the index hole is encountered on the diskette. This pulse should appear approximately every 166.67 milliseconds after the drive spindle has come up to speed. The Index pulse is used by the FDC chip to synchronize various command operations. Refer to the FD179x spec sheet for the details on how this signal is used.

This signal comes from Pin 9 of Multiplexer U17. It can be sourced from the drive logic of any internal or external drive by signal "IPI" or "IPE" which are tied to Pin 2Ø of the Drive Bus. The logic status of signal "INT*/EXT" (see same) at Pin 1 of U17 will determine the input selection.

TKØ*
(TP 17)

To Pin 34 of FDC U18. This is the Track Ø signal. A logic low at this input is used to inform the FDC chip that the Read/Write head is positioned over Track Ø.

This signal comes from Pin 12 of Multiplexer U17. It can be sourced from the drive logic of any internal or external drive by signal "TRKØI" or "TRKØE" which are tied to Pin 42 of the Drive Bus. The logic status of signal "INT*/EXT" (see same) at Pin 1 of U17 will determine the input selection.

WD

From Pin 31 of FDC U18. This is the Write Data signal to the drive. The signal at this Pin will be a 2ØØ nanosecond (MFM) or 5ØØ nanosecond (FM) output pulse. Each output pulse will produce a flux transition on the diskette media. This output is a serial pulse train of bits representing address marks as well as data and clock information in both the FM and MFM formats.

Signal "WD" is applied to Pin 1 of U28. It will emerge at Pin 6 of U28 as the Write Precompensated Data signal to the drive. See signal "WRDATA*".

EARLY — From Pin 17 of FDC U18. This is the early signal for Write Precompensation. When this signal is asserted along with the Write Data pulse appearing at Pin 31, signal "EARLY" will cause U28 to shift the Write Data pulse early for Write Precompensation. See signal "WRDATA*".

LATE — From Pin 18 of FDC U18. This is the late signal for Write Precompensation. When this signal is asserted along with the Write Data pulse appearing at Pin 31, signal "LATE" will cause U28 to shift the Write Data pulse late for Write Precompensation. See signal "WRDATA*".

VFOE*
WF — From, or to Pin 33 of FDC U18. This is a bi-directional signal.

During a Write operation, this signal will appear as an input to the FDC. The FDC will use this input to monitor any Write Faults detected by U28. A Write Fault condition will cause this normally high signal to switch to a logic low. The FDC will immediately terminate the Write operation when this logic low is sensed.

This signal will become an input to U28 when the FDC is performing a Read operation. It is used to enable the Read Data Clock Recovery circuits of U28. Signal "VFOE*" will remain low until the Read operation has reached the end of the Data Field.

RCLK
(TP 26) — From Pin 12 of U28. "RCLK" is used as the Data Recovery signal by the FDC.

In the Double Density mode of operation, the nominal "RCLK" signal will be a divide-by-8 of the VCO input frequency (for 8 inch drives, this will be 4 MHz), or 5ØØ KHz. The nominal "RCLK" frequency will be 25Ø KHz in the Single Density mode.

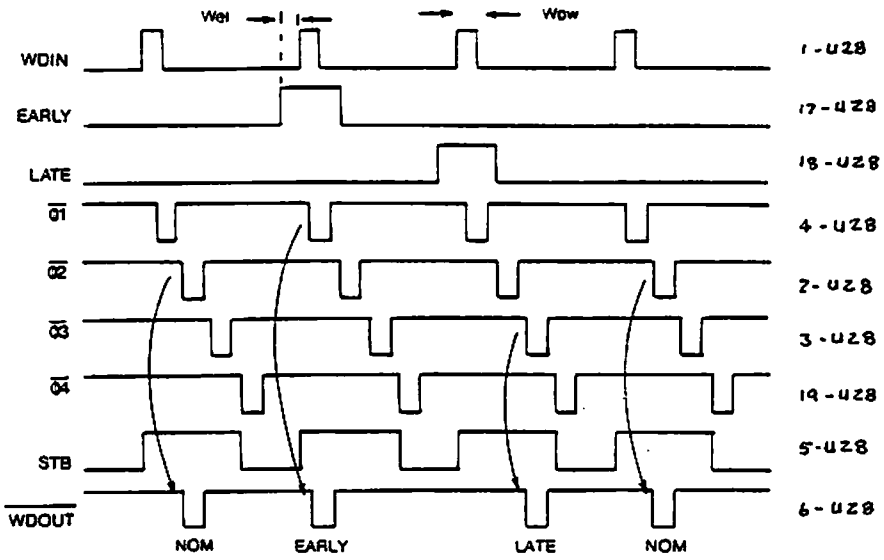
During a Read operation U28 will constantly monitor the phase relationship between the raw data input transitions at Pin 11 with the nominal "RCLK" frequency. The combined effort of U28 and U24 will cause the "RCLK" frequency to increase or decrease, depending on the phase relationship of these two signals.

When the transition of the Raw Data input occurs at the beginning of the nominal "RCLK" window, signal "PU" at Pin 13 of U28 will switch to a logic high and cause the VCO input frequency to increase. If the Raw Data input transition occurs at the end of the "RCLK" window, signal "PD" at Pin 14 will switch to a logic low and decrease the VCO frequency.

Should the Raw Data input transition occur at the center of the "RCLK" window, signals "PU" and "PD" will remain tri-stated, indicating that no adjustment of the VCO frequency is needed.

The resultant "phase corrected", or adjusted "RCLK" signal appearing at Pin 12 of U28 is applied to Pin 26 of the FDC chip. The basic function of this signal in the FDC is to latch in the Raw Data input signal appearing at Pin 27. Refer to the WD1691 spec sheet for a detailed functional description of this procedure.

WRDATA* From Pin 6 of U28. When the FDC is performing a Write operation, this signal will represent the serial, pre-compensated Write Data stream going to the drive. The Write Data will be pre-compensated, as determined by the FDC, only when signal "DDEN*" is at a logic low and signal "TG43" is at a logic high. The timing diagrams below presents an example on how the Write Data is pre-compensated.



Signal "WRDATA*" is applied to Pin 1 of One-Shot, U15. Note: label Pin 1 "WRDATA*", since it isn't labeled on the schematic.

One-Shot U15 is used to set the width of the Write Data pulses to 25Ø nanoseconds. The Write Data pulses from the one-shot are inverted at pins 8 and 6 of U7 to become the Internal and External Write Data signals "WDI*" and "WDE*", respectively. These signals are tied to Pin 38 of the Drive Bus.

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Glossary - Sheet 1

Only the mnemonics originating from Sheet 1 of the Revised FDC schematic will be covered under this heading.

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CLOCK — From Pin 44 of the Model II System Bus. This is the 4 MHz System clock. It is buffered at Pin 1Ø of U27 to become signal "CLOCKI" (see same).

Note: U27 is an open collector device. It will open, or switch to a high Z state with a logic high. Resistor R2 is used to pull-up the line to +5 volts.

CLOCKI — From Pin 1Ø of Buffer U27. This 4 MHz signal is applied to Pin 25 of PIO U12. The PIO will use this clock to synchronize certain internal signals.

This 4 MHz signal is also applied to Pin 11 of U26 where it is divided by 2 to emerge at Pin 9 as a 2 MHz signal. This 2 MHz signal is tied to Terminal "P", which is jumpered to Terminal "Q", to produce signal "FDCLK" (see same).

FDCLK (TP 18) — From Pin 9 of Divider U26: also see signal "CLOCKI".

This 2 MHz signal is used at Pin 11 of U35 as a continuous trigger. It will continually clock out the logic status appearing at Pin 12 of U35, to Pin 9 of U35. The resultant output signal is called "DDEN*" (see same).

Signal "FDCLK" is also applied to Pin 24 of FDC, U18/2. The FDC will use this 2 MHz signal as an internal timing reference.

DDEN* (TP 3Ø)

From Pin 9 of U35. This is the Double Density Enable signal. A logic low will enable the Double Density mode.

The Double Density Enable signal will be asserted when the CPU does a Write to Port EF with Data Bit 7 set. The resultant signal appearing at Pin 12 of U35 will be clocked out by signal "FDCLK" (see same) to produce signal "DDEN*".

This signal is used at Pin 37 of FDC U18/2. When asserted, signal "DDEN*" will set the Interface Control logic of the FDC. This logic level will enable the double density circuits of the chip.

Signal "DDEN*" is also applied to Pin 15 of U28/2. The primary use of this signal at U28/2 is to select the correct VCO frequency of operation. When this signal is asserted, the internal timing and control signals of U28 will be referenced directly by the 4 MHz VCO signal appearing at Pin 16.

Signal "DDEN*" will be negated in the Single Density mode of operation. The logic high state of signal "DDEN*" in this operational mode will be used to enable a divider in U28. This divider will change the internal VCO frequency to 2 MHz. As a special note, signal "RCLK" (see same) will have a frequency of 25Ø KHz in this mode of operation.

MOTORON*

From Pin 12 of U25. It is not currently used in the Model II, and would be used only if the FDC Board were interfaced to 5-inch drives. It would be asserted when any one of the drive select signals appearing at pins 1, 4, 5, or 2 of U1 is at a logic low.

Signal "MOTORON*" is used in the servo drive logic of the drive. An asserted low signal will turn on the drive motor. This signal is connected to Pin 16 of the 5 inch drive connectors, J1 and J2. Note: J1 is incorrectly labeled on the schematic as J3. Change it to J1.

Signal "MOTORON*" is also tied to Terminal "A" on sheet 2 of the schematic. If the FDC Board is interfaced with a 5-inch drive, this signal must be jumpered to Terminal "B" to provide the necessary "Ready" signal to the FDC chip. This is a false Ready signal to the FDC. With 5-inch drives, we can only assume that the drive will be ready for a Read or Write operation as soon as the drive is selected.

As a special note, the software drive routine will introduce a delay of approximately 1 second before the Read or Write operation is actually initiated. This delay will allow the drive motor to come up to speed.

INT*/EXT From Terminal "T". The source of this signal is programmable. The jumper options are shown below.

* Terminal "T" to Terminal "U": One internal drive.

  The source for signal "INT*/EXT" will come from Pin 2 of U36 with this option.

* Terminal "T" to Terminal "S": Two thinline internal drives. Terminal "H" must also be jumpered to Terminal "F".

  The source for signal "INT*/EXT" will come from Pin 6 of U5 with this option.

Signal "INT*/EXT" is used at Pin 1 of Multiplexer, U17/2. When this signal is a logic low, the Ready, Write Protect, Index Pulse, and Track Ø Status signals of the internal drive(s) will be routed out at pins 4, 7, 9, and 12, of U17/2.

Signal "INT*/EXT" is also applied to Pin 1 of Multiplexer U16. When this signal is a logic low, the Raw Data, Two Sided, and Disk Change signals of the internal drive(s) will be routed out at pins 4, 7, and 9, of U16. These input signals are further explained on the next page.

* Raw Data.....This is the Raw Read Data from the drive. It is routed to Pin 1Ø of One-Shot U6. Note: The "B" input of U6 is Pin 1Ø. Label it.

  The output of the one-shot will produce a 25Ø nanosecond pulse with every data input transition. This output line is called "RDATA*" (see same).

* Two Sided.....This is an optional signal that is available from a double sided diskette. A second Index LED sensor is used by the drive to detect when a double sided diskette is installed.

  The Two Sided signal will be at a logic low when a double sided diskette is in use.

  The logic status of the two sided signal is routed to Pin 14 of PIO U12 where it is called "TWOSID" (see same).

* Disk Change.....This signal will become asserted, or switch to a logic low when the diskette is changed or when the drive door lever lock is open.

  The exact logic used to generate this signal will depend on the type of drive that is in use.

  The logic status of this signal is routed to Pin 13 of PIO U12 where it is called "DSKCHG" (see same).

RDATA* (TP 29) From Pin 12 of One-Shot U6. This is the Raw Data signal originating from the drive. The one-shot will produce a negative-going 25Ø nanosecond pulse with every positive-going data input transition at Pin 1Ø. Note: The "B" input of U6 is Pin 1Ø. Label it.

This signal is applied to Pin 11 of U28/2 where it will be used to control the frequency of "RCLK" (see same).

The "RDATA*" signal is also routed to Pin 27 of FDC, U18/2. The serial Read information appearing at this input will be latched (through the "RCLK" window) into the Data Shift Register of the FDC. The FDC will execute signal "DRQ" (see same) when this Register is loaded.

TWOSID — To Pin 14 of PIO U12. This is the optional double-sided diskette detect signal originating from the drive. This signal is not only optional, but also conditional, since its availability will be determined by the type of drive that is in use. More on how this signal is produced is covered under signal "INT*/EXT".

How this signal is monitored at the "A" Port of the PIO will depend on the TRSDOS® version in use. It is safe to say that this was considered a "don't care" signal prior to version 4.x of TRSDOS®. TRSDOS® 4.x was written to support the introduction of double-sided thinline drives into the System's line.

Signal "TWOSID" will normally be at a logic low, and will switch to a logic high only when a double-sided diskette is installed in the appropriate drive.

Note 1: U16 functions not only as a multiplexer, but also as an inverter. The bubbles at pins 4, 7, and 9 imply that the output signals are asserted low, when in fact they are simply inversions of the inputs.

Note 2: Just exactly how the PIO is programmed to service the Status signals at the input of the "A" Port is uncertain at this time. It is logical to assume however, that the PIO could be programmed to support Mode 3 Interrupts (bit input/output). In this mode of operation, the PIO will generate an Interrupt Request whenever any one of the input Status signals at the "A" Port changes its logic state. Again, the System may be programmed to just check the status of these signals periodically, by polling. As a third assumption, some of the Status signals (namely, "FDCINT") could be programmed to generate Interrupts, while the others are just polled.

DSKCHG — To Pin 13 of PIO U12. This is the Disk Change detect signal originating from the drive. More on how this signal is produced is covered under signal "INT*/EXT". Also see signal "TWOSID" for supporting information.

PRIME — From Pin 12 of PIO U12. This is an optional Software Reset signal to the printer, and is functionally identical to a Power On Reset. This signal is not in use at this time. There should be no jumper between terminals JPD and JPE.

An asserted "PRIME" signal would appear as a logic low at Pin 8 of Inverter U3.

FAULT — To Pin 1Ø of PIO U12. This is the Fault Detect signal from the printer. The exact fault conditions that will cause this signal to be present will depend on the type of printer in use. As an example, the DW II printer will execute this signal whenever an error is detected in the Select or Space servo circuits, or when the printer runs out of ribbon.

An asserted "FAULT" signal will appear as a logic low at Pin 1Ø of the PIO. The System will not attempt to load data to the printer when this signal is asserted.

Note: When no printer is interfaced to the System, Resistor R5 will keep the line at Pin 11 of U3 in the Fault state for the reason mentioned above.

SEL — To Pin 9 of PIO U12. Note: This signal is incorrectly labeled "DEL". Change this to "SEL".

"SEL" is an optional signal from the printer. Its logic status is usually controlled by the On Line/Off Line switch located on the printer's console.

An On Line condition will place a logic low at Pin 9 of the PIO.

PE — To Pin 8 of PIO U12. This is the optional Paper Empty signal from the printer.

A Paper Empty condition will place a logic high at Pin 8 of the PIO.

Note: When no printer is interfaced to the System, Resistor R12 will keep the line at Pin 6 of U9 in the Paper Empty state. This condition will prevent the System from trying to load the printer Port with data.

BUSY (TP 1Ø) — To Pin 7 of PIO U12. This signal will be asserted at a logic high when the printer is not ready.

The conditions which will cause the printer to execute this signal will depend on the type of printer. Some of the conditions that could generate this signal are listed below.

* Data in Buffer.
* Reset state.
* Off Line mode.
* Printer circuits in error.
* Out of ribbon.
* Printer cover open.

Note: When no printer is interfaced to the System, Resistor R4 will keep the line at Pin 1Ø of U9 in the Busy state. This condition will prevent the System from trying to load the printer Port with data.

PACK* — From Pin 19 of the of the printer connector.

Signal "PACK*" is a 5 to 1Ø microsecond negative-going pulse from the printer. An asserted "PACK*" signal is an indication that the previous byte of data from the PIO has been loaded into the Buffer of the printer. This signal is also used to inform the PIO that the printer is ready for another data byte transfer.

The "PACK*" signal is buffered at Pin 6 of U13, from where it is applied to Pin 17 of the PIO. Pin 17 is the B Strobe input of the PIO.

PSTROBE* (TP 2) — From Pin 4 of One-Shot U6. To Pin 1 of the printer connector.

Signal "PSTROBE*" will be generated a few nanoseconds after the valid ASCII data to the printer appears at the "B" Port of the PIO. This 1.5 microsecond negative-going pulse is used to latch in the ASCII data byte into the Buffer of the printer.

"PSTROBE*" originates from Pin 21 of the PIO. This is the B Ready output of the PIO. The B Ready signal is normally at a logic low and will switch to a logic high only when the "B" Port Output Register is loaded with an ASCII byte of data from the CPU. One-Shot U6 will generate signal "PSTROBE*" when Pin 21 of the PIO switches to a logic high.

IORQI* — To Pin 36 of PIO U12. From Pin 3 of Buffer U33/2.

Signal "IORQ*" will be asserted when the CPU is in the process of reading or writing to a Port, or when the CPU is in the process of acknowledging an Interrupt Request. "IORQ*" is used at the PIO in conjunction with signal "SYNCI*" as an Interrupt Acknowledge from the CPU.

INTRQI* (TP 5) — From Pin 23 of PIO U12. To Pin 9 of U27 where it is buffered at Pin 8 to become signal "INTRQ*". Signal "INTRQ*" is applied to Pin 11 of the Model II System Bus where it will travel back to Pin 11 of the CPU Board and end up at the "INT*" input of the CPU.

Signal "INTRQI*" is the Interrupt Request signal from the PIO. The conditions which will execute this signal will depend on how the PIO is programmed to service interrupts. See signals "FDCINT", "TWOSID", "DSKCHG", "FAULT", "SEL", "PE", and "BUSY" for supporting information.

RDI* — To Pin 35 of PIO U12. From Pin 7 of Buffer U33/2. When this signal is asserted as a logic low, it will indicate that the CPU is in the process of performing a Memory Read or I/O Read operation. The Read signal is used in conjunction with signals "B/A* Select", "C/D* Select", "CE*", and "IORQ*" to transfer data from the PIO to the CPU.

M1* To Pin 37 of PIO U12. This Pin will be at a logic low when activated by signal "SYNCI*" or signal "RESETI*".

Signal "M1*" has four functions:

* When asserted, this signal will be used to synchronize the PIO interrupt logic.

* When this signal appears without signals "RDI*" and "IORQI*", it will be used to reset the PIO.

* When asserted with signal "RDI*", the PIO is being informed that the CPU is in the process of performing a Memory Read operation.

* When asserted along with signal "IORQI*", it will be used to inform the PIO that the CPU is in the process of acknowledging an Interrupt.

"RESETI*" is the System reset signal from Pin 13 of Buffer U33/2.

"SYNCI*" is the M1 signal from the CPU at Pin 11 of Buffer U33/2.

B/A* To Pin 6 of PIO U12. From Address Line, AØI.

This is the PIO "B" Port or "A" Port select signal. The logic status of this signal will define which Port will be accessed during a data transfer between the PIO and CPU.

A logic low at this input will select the "A" Port of the PIO. This selection is an indication that the CPU is in the process of reading Port EØ to check the FDC and Printer Status signals.

The "B" Port of the PIO will be selected when Pin 6 is at a logic high. This selection is an indication that the CPU is in the process of writing to Port E1 of the PIO. The CPU will load the "B" Output Register with ASCII data for the printer during this write.

C/D* To Pin 5 of PIO U12. From Address Line, AlI. This is the PIO Control or Data select signal.

A logic high on this Pin during a CPU Write to Port E2 will be interpreted by the PIO as a control, or command signal used for the configuring of the "A" Port. The "B" Port of the PIO will be "commanded", or configured when the CPU is writing to Port E3.

When this signal is a logic low at Pin 5, the PIO will decode this logic status as a Data Select signal, indicating that the CPU is in the process of transfering data between the CPU and the "A" or "B" Ports of the PIO. The transfer Port will depend on the logic status of signal "B/A*" (see same).

==========

Jumper Configuration Table

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Standard Configuration	
Installed Jumpers	**Function**
B to C	8-inch drive ready signal
J to K	E0H-EFH port addressing
L to M	active high XFERRQ
P to Q	2-MHz FDC clock
T to U	drive 0 INT*/EXT select

Optional Configuration	
Installed Jumpers	**Function**
D to E	prime signal to printer
Q to R	1 MHz FDC clock
M to N	active low XFERRQ
I to J	A0H-AFH port addressing
A to B	mini-drive ready signal
H to F, S to T	Two internal mini-drives INT*/EXT select

FDC Board Test Points

TP 1	Drive Ø Select.....Pin 2 of U36/1. This test point is not shown on the schematic.
TP 2	PSTROBE*.....Pin 4 of U6/1.
TP 3	READY.....Pin 2 of U2/2.
TP 4	HLT.....Pin 23 of U18/2.
TP 5	INTRQI*.....Pin 23 of U12/1.
TP 6	DIR.....Pin 16 of U18/2.
TP 7	SOFTMR*.....Pin 11 of U14/2.
TP 8	CEFDC*.....Pins 5, 6, 7, and 9 of U23/2.
TP 9	STEP.....Pin 15 of U18/2.
TP 1Ø	BUSY.....Pin 7 of U12/1.

TP 11 CEPIO*.....Pins 1, 2, 3, and 4 of U23/2.

TP 12 FDCINT.....Pin 39 of U18/2.

TP 13 IP*.....Pin 9 of U17/2.

TP 14 From Pin 4 of U2/1.

A logic high indicates that the Drivers of U2Ø and U19 are selected for an FDC Read.

TP 15 OUT*.....Pin 6 of U34/2.

TP 16 Pin 13 of U15/2.

A positive-going 25Ø nanosecond pulse representing the transition of one Write Data Bit.

TP 17 TRØ*.....Pin 12 of U17/2.

TP 18 FDCLK.....Pin 9 of U26/1.

TP 19 WPRI*.....Pin 7 of U17/2.

TP 2Ø DRSEL*.....Pin 8 of U22/2.

TP 21 Pin 17 of U29/2.

The voltage at this Pin will set the width of the four output pulses of the 4-Phase Clock U29. The DC voltage at this test point will vary from Ø to approximately 1Ø volts, depending on the setting of Potentiometer, R3. See TP 27.

TP 22 DRQ.....Pin 38 of U18/2.

TP 23 CPUIN.....Pin 1Ø of U2/2.

TP 24 RESETI*.....Pin 13 of U33/2.

This is the System Reset signal from the CPU Board. A logic low indicates that a System Reset is in progress.

TP 25 Pin 2 of U24/2.

The voltage at this test point should be 1.4 volts DC. Potentiometer R2 is used to set this voltage when the drive is inactive. This adjustment is part of the FDC Board alignment procedure.

TP 26 RCLK.....Pin 12 of U28/2.

TP 27 Pin 7 of U29/2. Also see TP 21.

This is the Ø-Phase negative-going output signal of the 4-Phase Clock U29. This pulse is adjusted to a width of 25Ø nanoseconds with Potentiometer, R3. This adjustment must be performed while the FDC is in the process of writing to a drive track greater than Track 43.

TP 28 HLD*.....Pin 6 of U2/2.

TP 29 RDD*.....Pin 12 of U6/1.

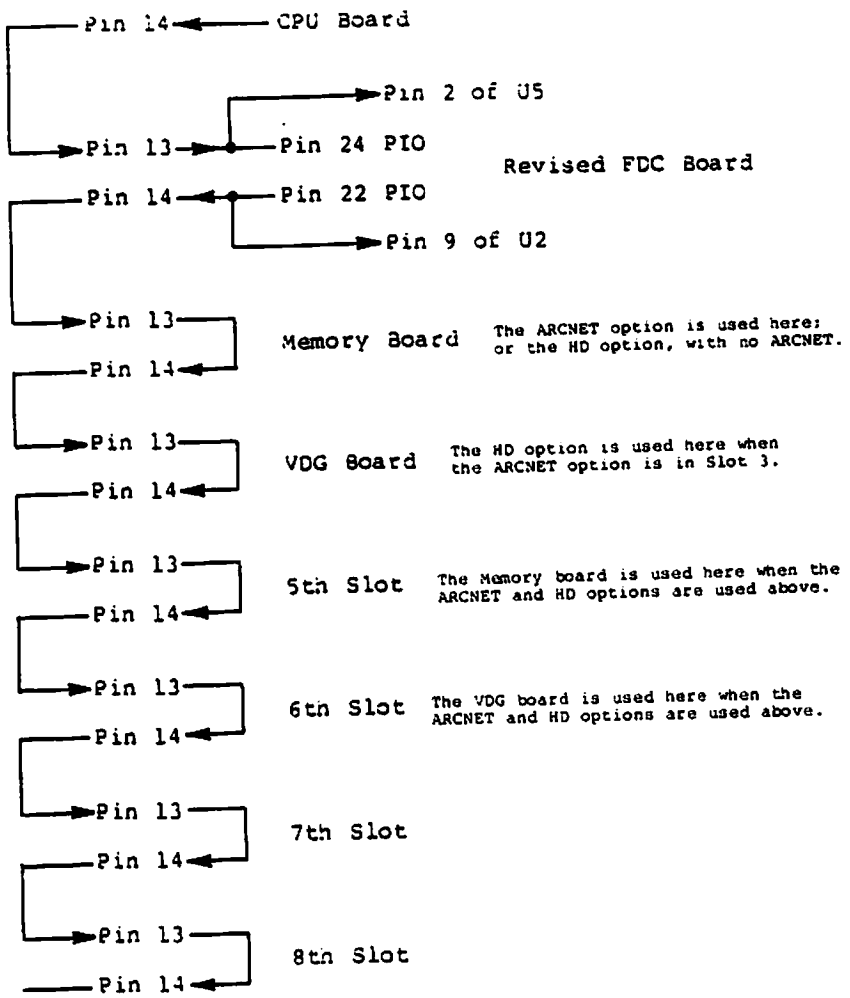
TP 3Ø DDEN*.....Pin 9 of U35/1.

TP 31 IN*.....Pin 8 of U34/2.

TP 32 Regulated +5 volts DC.

TP 33 + 12 volts DC from pins 77 and 78 of the System Bus.

Mother Board Interrupt Loop



Note: All boards with devices tied to the interrupt loop must occupy slots adjacent to each other. This must be done to keep the interrupt chain intact. The farthest board from the CPU board will have the lowest interrupt priority.

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Section Four

Model II VDG Board

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Contents

The listings in this glossary are divided into 2 sections, respective to the two sheets of the VDG schematic.

When a signal from one sheet is referenced to another, a pointer, "/#", will be used to indicate the sheet: i.e. From Pin 6 of U29/2 To Pin 26 of U11/1.

The VDG schematics reflect the circuits which are on the REV B Board. The REV A and REV C Boards have only minor differences.

Index for VDG Board Signals

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Glossary - Sheet 1

Only the mnemonics originating from Sheet 1
of the VDG schematic will be
covered under this heading.

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RCLOCK
(TP 18)

From Pin 6 of Buffer U1. To Pin 9 of Inverter U1, Pin 11 of U17, and TP 18. This is the 12.48 MHz signal from the master oscillator. This frequency has a period of 80.1282 nanoseconds.

To Pin 9 of U1 where it is inverted to become signal "RCLOCK*" (see same).

To TP 18 where it becomes the first of four optional signals which can be used to adjust the video display for clarity and sharpness.

To Pin 11 of U17 where it is divided by two. The frequency at Pin 9 of U17 is 6.24 MHz.

RCLOCK*
(TP 20)

From Pin 8 of Inverter U1. To Pin 13 of U1 (this Pin is labeled "18" on the schematic: change it to Pin "13"), To Pin 5 of U28, and To TP 20.

Signal "RCLOCK*" is not only the inverted result of signal "RCLOCK", but it is also delayed by approximately 4 nanoseconds, due to the propagational characteristics of the chip.

To Pin 13 of U1 where it is inverted to become signal "RCLOCKP" (see same).

To Pin 5 of U28 where it is gated through the logic to become signal "CLOCK" (see same) in the 80-Character Display mode.

To TP 20 where it becomes the second of four optional signals which can be used to adjust the video display for clarity and sharpness.

RCLOCKP (TP 19) — From Pin 12 of U1. To Pin 11 of U1, and to TP 19. This signal has the same frequency as as signal "RCLOCK" (see same) but it is now displaced in phase with respect to "RCLOCK" by approximately 12 nanoseconds. This phase displacement is due to the combined inverter propagational characteristics.

To Pin 11 of U1 where it is inverted to become signal "RCLOCKP*" (see same).

TO TP 19 where it becomes the third of four optional signals which can be used to adjust the video display for clarity and sharpness.

RCLOCKP* (TP 17) — From Pin 10 of U1. To TP 17 where it becomes the fourth of four optional signals which can be used to adjust the video display for clarity and sharpness. Because of the combined propagational characteristics of the inverters, signal "RCLOCKP*" will be inverted and displaced with respect to signal "RCLOCK" by approximately 16 nanoseconds.

Note: The displacement figures given on the four signals mentioned above are based on measured values. The propagation delays will differ with different VDG Boards because the electrical characteristics of the chips will never be exactly the same.

CLOCK (TP 26) — From Pin 8 of U28. This signal will have a frequency of 12.48 MHz in the 80-Character Display mode, or 6.24 MHz in the 40-Character Display mode. The controlling signal is "80*/40 CHAR EN" at Pins 1, 2, and 13 of U28. Signal "CLOCK" will have a frequency of of 12.48 MHz when signal "80*/40 CHAR EN" is at a logic low.

Signal "CLOCK" is routed to Pin 4 of Gate U3, Pin 11 of Inverter U33, and to Pin 2 of Presettable Counter U26.

Signal "CLOCK" is inverted at Pin 11 of Gate U33, to become signal "DCLK".(see same).

At Pin 4 of Gate U3, signal "CLOCK" is gated with signal "TCLK*" (see same) to produce signal "PLCLK*" (see same). This gating action synchronizes signal "PLCLK*" to signal "CLOCK".

The final use of signal "CLOCK" is as a clock to Presettable Counter U26.

Understanding the Presettable Counter U26.

This explanation is based on the assumption that the VDG is operating in the 8Ø-Character Display mode.

U26 is a high speed 4-bit binary counter, preset to a count of eight by the hard-wired binary 9 at pins 3, 4, 5, and 6. It is positive edge-triggered at Pin 2 by signal "CLOCK". The TC, or Terminal Count ouput line (this is Pin 15: it is not labeled on the schematic) will produce a positive-going 8Ø.1282 nanosecond pulse when all of the Q outputs of the counter are high. The frequency of the TC pulse will be one-eigth that of the clock input. The pulse repetition time of the TC pulse will be eight times that of the clock period, or 641.Ø26 nanoseconds.

The output frequency of the Q1 line is 3.12 MHz. This line produces signal "Q1" (see same) where it will be used in the CPU Wait logic.

Signal "CCLK" (see same) is the product of the Q2 output. It has a frequency of 1.56 MHz in the 8Ø-Character mode.

When the Q outputs of the counter are all high, the next clock will reset all of the outputs to a logic low. At this moment, the logic low on the Q3 line will load the hard-wired binary 9 into the counter. This load will cause the rising edge of the next clock pulse to preset the count of the Q output lines to a binary 9.

Q1 — From Pin 13 of Presettable Counter U26. To Pin 9 of U2/2. This signal is ANDed with signal "MSELP" (see same) at U2/2 to limit the period of signal "WAIT" (see same) to approximately 16Ø nanoseconds.

CCLK — From Pin 12 of Presettable Counter U26. This signal will have a frequency of 1.56 MHz in the 8Ø-Character Display mode. It is routed to Pin 21 of U11 where it becomes the character clock of the CRTC. The transparent width of one Character Display column is based on the period of this signal.

Signal "CCLK" is also used as a clock at Pin 6 of U32/2.

TCLK* — From Pin 12 of Inverter U33. In the 8Ø-Character Display mode, this signal will be a negative-going

80.1282 nanosecond pulse with a repetition time of 641.026 nanoseconds. It is used as a clock at Pin 11 of U8 to latch the ASCII data from the video RAMs into the character generator ROM. The repetition time of signal "TCLK*" is the width of one display column.

PLCLK* — From Pin 6 of U3. This is the "TCLK*" (see same) signal which has been synchronized to signal "CLOCK". It is used at Pin 1 of U10 to load in the video dot information from the character generator ROM.

DCLK — From Pin 10 of Inverter U33. This signal is the inversion of signal "CLOCK" (see same). It is used at Pin 2 of U10 to serially shift the video dot information out to Pin 9.

TADCLK — From Pin 3 of U29. This is the TC signal out of Presettable Counter U26, which has been synchronized to signal "DCLK". This is the Transfer Address Clock. It is used at Pin 9 of the Timing Latch U12.

VSYNC (TP 6) (TP 15) — From Pin 40 of CRTC U11. This is the Vertical Sync Pulse. Its positive-going pulse has a repetition rate of 16.67 milliseconds, or frequency of 60 Hz.

The width of this sync pulse is a dependent variable of the programmed horizontal scan rate. The CRTC will always set the width of this pulse to 16 times that of the programmed rate of the horizontal scan. See "HSYNC". The pulse width of this signal is about 1 millisecond.

This sync signal is sent to Pin 1 of U4 to be inverted and buffered before it is routed to the video monitor. The sync pulse is used in the monitor to synchronize the the vertical deflection oscillator to the vertical scan rate of the VDG.

"VSYNC" is also used at Pin 3 of U16/2 which is part of the Real Time Clock logic. See "NMIRQ*"

HSYNC (TP 5) — From Pin 39 of CRTC U11. This is the Horizontal Sync Pulse. The width and repetition rate of this signal is set to the programmed values contained in CRTC Horizontal Timing Registers, R0 and R1. Refer to the specification sheet of the 6845 CRTC for details.

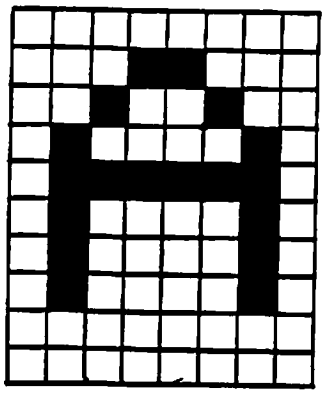
In this application, the "HSYNC" signal is a 5 microsecond positive-going pulse with a repetition rate of 64 microseconds, or a frequency of approximately 15600 Hz.

This sync signal is used at Pin 5 of One-Shot U5 as a trigger. The purpose of this one shot is to stretch, or increase the width of the sync pulse to approximately 27 microseconds. The increase in width provides noise immunity and pulse width stability of the sync. This stretched pulse is call "CHSYNC" (see same).

VOUT (TP 12) — From Pin 9 of Shift Register U10. This is the video output line. This video dot, or pixel information, is sent out serially to Pin 9 of U4 where it is Exclusive ORed at Pin 10 with signals "DCURSOR" (see same) and "DREVID" (see same).

Note: In the 80-Column by 24-Row Display format, the display area of the video screen will contain 1920 primary display cells. The primary cells are made up of the various Column - Row address combinations which make up the total display area of the screen.

A primary display cell will occupy an area on the display screen which is 8 dots wide and 10 lines deep. This is illustrated by the drawing below.



Note that the illustration in the Model II Technical Reference Manual is incorrect.

The display screen will be illuminated only when "VOUT" is at a logic high.

DISPEN (TP 3)

From Pin 18 of CRTC U11. This is the Display Enable signal. This signal will be asserted when the CRTC is providing the Column - Row addressing to the video RAMs. In other words, this signal will be asserted only within the 8Ø-Column by 24-Row Display area.

"DISPEN" is routed to Pin 3 of U15. This chip will block the display enable signal under the two following conditions.

* When signal "MSELP*" is asserted at Pin 4 of U15. Signal "MSELP*" will be asserted when the CPU is in the process of accessing the video RAMs. The Display Enable signal is blocked during this access time to prevent spurious video information from appearing on the display screen.

  Note: Under normal TRSDOS® operation, the CPU is allowed to access the video RAMs only when the VDG is within the vertical blanking interval of the video timing matrix.

* When signal "BLNKVID*" is asserted at Pin 5 of U15.

  Signal "BLNKVID*" can be controlled through software by writing to Port FF with Data Bit 6 set to a logic high. This signal will blank the entire display screen when it is asserted.

CURSOR

From Pin 19 of CRTC U11. To Pin 4 of Timing Latch U12. U12 is wired to delay this signal by two column periods. This delayed cursor signal is called "DCURSOR" at Pin 12 of U12.

Signal "DCURSOR" is routed to Pin 12 of U4, then on to Pin 1Ø of U4 where it is Exclusive ORed with the video dot information at Pin 9.

Note: Converting the ASCII data from the video RAMs into what is seen on the display screen requires a lot more processing than most of the other signals that are produced by the VDG. Because of this, signal delays are introduced which must be corrected before the video information appears on the screen. The cursor signal is one of three signals which are delayed to bring it into the right phase with respect to the video dot information.

The cursor is the blinking display cell that is seen on the screen: it is a pointer. Under TRSDOS® operation, various function and control keys can be used to turn on a blinking cursor, turn off the cursor, turn on a steady cursor, etc. The cursor can be positioned into any of the display cells with the Up, Down, Right, and Left arrow keys. A keyboard entry will always be placed in the display cell that is presently occupied by the cursor. Refer to the Model II User's Manual for additional information.

CHSYNC (TP 4) — From Pin 6 of U5. This is the stretched Horizontal Sync Pulse. See "HSYNC". This signal goes to Pin 4 of Buffer U4. The buffered sync pulse at Pin 6 of U4 is then routed to the video monitor where it is used to synchronize the horizontal deflection oscillator to the horizontal scan rate of the VDG.

REVID — From Pin 9 of U8. This is the Reverse Video signal. Signal "REVID" is applied to Pin 6 of Timing Latch U12, which will delay this signal by one column period to bring it into the proper phase relationship with the rest of the video signals. This delayed signal is called "DREVID" at Pin 7 of U12, and is Exclusive ORed at Pin 13 of U4 with signal "DCURSOR".

This signal is programmer controllable. A TRSDOS® Control Z code will place the Model II in the Reverse Display, or Black-on-White Mode. The display will remain in this mode until it is reset by the programmer. A TRSDOS® Control Y code will return the display to it's Normal, or White-On-Black Mode.

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Glossary - Sheet 2

Only the mnemonics originating from Sheet 2 of the VDG schematic will be covered under this heading.

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IOADSEL* From Pin 8 of Port Decoder Gate U27. This signal will be asserted when the CPU is in the process of addressing Ports FC through FF.

This signal is inverted at Pin 12 of U3Ø, then on to Pin 9 of U13 where it is ANDed with signal "IOCYC" (see same) to produce signal "IOSEL"(see same).

Note: U27 is a Multiple-Input Nand Gate.

Change input Pin 1Ø on the schematic to input Pin 1.

Change input Pin 17 on the schematic to input Pin 12.

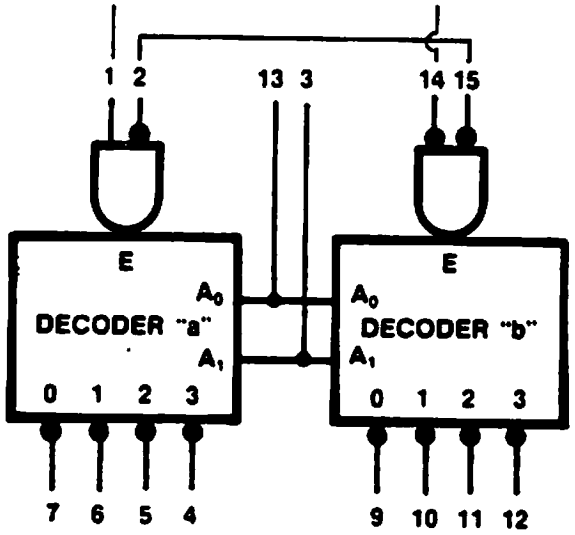
There is also a mistake in the foil pattern of the REV A and B Boards - the foil is actually connected to Pin 1Ø as shown on the schematic. Since Pin 1Ø is not used by the chip, the foil connection is made to Pin 1 by bridging Pin 1Ø to Pin 1 with a short piece of KYNAR wire. Refer to Technical Bulletin II:18 for details. The foil pattern on the REV C Board (and later Boards) is correct.

IOCYC From Pin 5 of Inverter/Buffer U4Ø/1. This signal is from the CPU Board. When asserted, this signal indicates that the CPU is in the process of executing an I/O Read or Write operation, and that the lower half of the Address Bus holds a valid I/O address.

Through U2 and U31 To Pin 1Ø of U13 where it is ANDed with inverted signal "IOADSEL*" (see same).

To Pin 13 of U2 where it is ANDed with signal "RD" (see same). This result is used at the Enable Pin of U31 (see below).

To Pin 1 of the Dual 2-Line To 4-Line Decoder/Multiplexer U31. The functional diagram of this chip is illustrated below to help clarify the poorly labeled block symbol shown on the schematic. ADØ goes to Pin 13, AD1 to Pin 3.



Vcc = Pin 16
GND = Pin 8

RD

From Pin 7 of Inverter/Buffer U4Ø/1. When this signal is asserted, it indicates that the CPU is in the process of reading data from Memory or an I/O device. In this application, it signifies a Read from an I/O device.

To Pin 12 of U2 where it is ANDed with signal "IOCYC" (see same).

To Pin 2 of U13 where it is ANDed with signal "IOSEL" (see same) to produce signal "IOBIE" (see same).

To Pin 13 of U13 where it is ANDed with signal "MSP" to produce signal "VRD" (see same) at Pin 11 of U13.

To Pin 1 of U3Ø/1 where it is inverted to become signal "RD*". This signal is ORed at Pin 12 of U42/1, where it becomes the Enable signal for CRTC U11/1. When this signal is asserted at Pin 23, it will enable the Internal Output Data Buffers of the CRTC.

IOSEL — From Pin 8 of AND Gate U13. This signal is the ANDed result of signals "IOCYC" and "IOADSEL*". It is applied to Pin 6 of NOR Gate U14 to generate signal "SELECT*" (see same).

IOBIE (TP 22) — From Pin 3 of AND Gate U13. This is the IO Bus Input Enable signal. It will be asserted when the CPU is in the process of reading Ports FC through FF. It is used to enable the Data Bus Drivers of U34 and U35.

WR — From Pin 9 of Inverter/Buffer U40/1. When this signal is asserted, it indicates that the CPU is in the process of writing data to Memory or to an I/O device.

To Pin 9 of U30/1 where it is inverted to become signal "WR*" (see same). This signal is ORed at Pin 13 of U42/1 where it becomes the Enable signal for CRTC, U11/1. When this signal is asserted at Pin 23, it will enable the Internal Input Data Buffers of the CRTC.

To Pin 1 of U2 where it is NANDed to signal "IOSEL" (see same) to produce signal "IOBOE*" (see same).

To Pin 4 of U2 where it is NANDed with signal "MSP" (see same) to produce signal "VWR*" (see same).

WR* — From Pin 8 of Inverter U30.

To Pin 13 of U42/1, then further, to become the Enable signal for CRTC U11/1. This signal, when asserted, will enable the Internal Input Data Buffers of the CRTC.

To Pin 22 of CRTC U11/1. This is the "R/W*" Pin of the CRTC. The logic status of this signal will determine whether the Internal Register File of the CRTC gets written or read. A logic low signifies a Write condition.

To Pin 10 of U3 where it is ANDed with the logic low from Pin 4 of Port Decoder U31. The product of this is signal "FFWR*" (see same) at Pin 8 of U3.

To Pin 10 of U24/1 of the Address Multiplexer. This signal will appear at Pin 9 of U24/1 when the CPU is in the process of writing to the video RAMs. "WR*" is routed to Pin 10 of the video RAMs where it is used as a Write Enable signal. Note: U24 is located within

the block symbol of the bottom LS157 on sheet 1 of the schematic. Note: all three LS157's contain parts of U23, U24, and U25.

IOBOE* (TP 9) (TP 21) — From Pin 3 of NAND Gate U2. This is the IO Bus Output Enable signal. It will be asserted when the CPU is in the process of writing to Ports FC through FF. It is used to enable the Data Bus Receivers of U34 and U35.

6845CS* — From Pin 6 of U29. This is the Chip Select signal to the CRTC U11/1. This signal will be asserted when the CPU is in the process of writing to Ports FC or FD.

Note: The CPU will be loading data into the Address Register of the CRTC when it is writing to Port FC. The binary weight of this data is used to enable one of the eighteen R Registers contained within the CRTC.

When the CPU writes to Port FD, it will be loading video timing data into the R Register that has been enabled by the contents of the Address Register.

Pin 24 of the CRTC is the Register Select input. Bit Ø of the System Address Bus is connected to this Pin. When Port FC is being addressed, this bit will be at a logic low, used at the CRTC to enable the Address Register. An address to Port FD will make this bit a logic high and disable the Address Register.

MSEL* (TP 28) — From Pin 8 of Multiple-Input NAND Gate U41. This signal will be asserted when the CPU is in the process of addressing the video RAMs with a Read or Write.

Note: The last 2K of the System Address Space (F8ØØH through FFFFH) is shared by both the System DRAMs on the Memory Board, and the video RAMs of the VDG. This is an overlay of the Address Space. To prevent bus contention problems in this area, the Model II is equipped with hardware decoders which are controlled by TRSDOS®. The decoders are located on the Memory and VDG Boards.

The functional operation of these decoders is synonymous to that of an R-S Flip-Flop. That is, when one decoder is set, the other will reset. The setting and resetting of these decoders will be determined by the logic status of Data Bit 7 when the CPU is writing to Port FF. When this bit is high, it will set, or enable the decoder of the VDG. At this same time, it will reset, or disable the decoder on the Memory Board.

The decoder of the VDG will always be set by TRSDOS® just before the CPU accesses the video RAMs. TRSDOS® will reset this decoder when the CPU has completed the RAM access.

Signal "MSEL*" is inverted at Pin 6 of U3Ø to become signal "MSEL" (see same).

"MSEL*" is also applied to Pin 1 of U32 as a clock. The negative-going transition of this signal will clock the high at Pin 4 of this chip, out to Pin 15. This output is called signal "WAIT" (see same).

The final application of signal "MSEL*" is to place a logic low at Pin 12 of the second half of U32. A few nanoseconds later, Pin 9 of this chip will go to a logic high by the inverse of this signal. Within a period of 641 nanoseconds, the negative transition of signal "CCLK" (see same) will clock these logic levels out to produce signals "MSELP" and "MSELP*".

MSEL — From Pin 6 of U3Ø. This signal is the inverse of signal "MSEL*" (see same).

This signal is routed to Pin 9 of U32. See "MSEL*".

"MSEL" is also applied to Pin 5 of U14 where it is then inverted to become signal "SELECT*" (see same).

WAIT — From Pin 15 of U32. This signal will be asserted at the moment when the CPU begins its video RAM access.

To Pin 1 of U14 where it is inverted to become signal "WAIT*". This signal goes to the CPU. See note on the next page.

Note: The "WAIT*" signal is used to indicate to the CPU that the addressed Video Memory and interface devices are not ready for a data transfer. The CPU will continue to enter wait states for as long as this signal is asserted. In this application, the wait period is limited to approximately 160 nanoseconds by signal "Q1" (see same) at Pin 9 of U2. The signal at Pin 10 of U2 will be at a logic high when the CPU is in the process of accessing the video RAMs.

SELECT* From Pin 4 of U14. This signal is derived from either signal, "IOSEL" or "MSEL".

Note: An asserted "SELECT*" signal is used to signify that the CPU is in the process of performing a Memory operation. This operation indicates that the Address Bus presently holds a valid address for a Memory Read or Write.

This signal is also used to indicate when the CPU is in the process of performing an I/O operation. During this time, the lower half of the Address Bus will be holding a valid I/O address for an I/O Read or Write.

Signal "SELECT*" goes to Pin 43 of the Z80 System Bus. There is no indication that this signal is used by the Model II at any time.

MSP (TP 13) From Pin 6 of U13. This signal will be asserted when the CPU is in the process of addressing the video RAMs.

"MSP" is used at Pin 12 of U13 where it is ANDed with signal "RD" to produce signal "VRD" (see same).

Signal "MSP" is also used at Pin 5 of U2 where it is NANDed with signal "WR" to produce signal "VWR*" (see same).

This signal is also applied to Pin 6 of Multiplexers U24, U25, and U26. These chips are all contained within the LS157 block symbols located on sheet 1.

VRD (TP 24) From Pin 11 of U13. This signal will be asserted when the CPU is in the process of executing a Memory Read operation from the video RAMs. It is used at Pin 15 of U36/1 and U37/1 to enable the Data Drivers of these Buffers.

VWR* (TP 2) — From Pin 6 of U2. This signal will be asserted when the CPU is in the process of executing a Memory Write operation to the video RAMs. It is used at Pin 1 of U36/1 and U37/1 to enable the Data Receivers of these Buffers.

MSELP — From Pin 11 of U32. This signal will be asserted when the CPU is in the process of accessing the video RAMs. It is used at Pin 10 of the Wait Limit Gate U2. A logic high at this Pin will allow signal "Q1" (see same) to pass. "Q1" is used to limit the duration of the wait signal. See "WAIT".

Signal "MSELP" is also used at Pin 4 of U13 where it is ANDed with signal "MSEL" to produce signal "MSP".

MSELP* — From Pin 10 of U32. This signal will be asserted when the CPU is in the process of accessing the video RAMs. It is applied to Pin 4 of U15 where it is used to block the video output signal. This action prevents any spurious video information from appearing on the display screen during this access time.

KBIRQ* (TP 27) — From Pin 5 of U17. This is the Keyboard Interrupt Request signal. This signal will be asserted when the Keyboard generates the "End-Of-Data" pulse after the last bit of the ASCII key entry code is loaded into Shift Register U6.

This signal is applied to Pin 6 of U38 to become one of the four Status signals which is polled by the CPU when it does a Read to Port FF.

Signal "KBIRQ*" is also routed to Pin 42 of the Model II System Bus. This signal will end up at Pin 20 of CTC U19 on the CPU Board.

Note: The CTC is a Four-Channel Counter/Timer. The four channels of this device can be individually programmed to handle the timing and counting applications required by the System.

In the Model II, the first three channels of the CTC are programmed as Timers. The output lines supply the timing signals required by the SIO.

The fourth channel is programmed as a counter which is set to a count of one. When the keyboard generates an Interrupt Request, signal "KBIRQ*" will be asserted and decrement this count to zero. This zero count will cause the CTC to trigger an Interrupt Request to the CPU. When the CPU acknowledges this Interrupt Request, the CTC will place the keyboard Interrupt vector on the Data Bus. This vector is a low-byte address which is added to the high-byte contained in the Interrupt Page Address Register of the CPU. This combination is the start address of the Keyboard Interrupt Request Service subroutine.

The service routine will cause the CPU to read Port FC and move the keyboard data into memory. Before returning to the main program, this subroutine will re-initialize the CTC counter to a one to prepare it for the next keyboard Interrupt Request.

FCRD* (TP 8) From Pin 9 of Decoder U31.

To Pins 1 and 19 of Buffer U7 where it is used to load the keyboard byte from Shift Register U6 into Memory.

This signal is also applied to Pin 4 of U17 where it used to set Pin 5 of this chip to a logic high. This will clear the keyboard Interrupt Request signal.

NMIRQ* From Pin 1Ø of U14.

To Pin 12 of the Model II System Bus. This is the Non-Maskable Interrupt Request signal from the Real Time Clock logic.

The Real Time Clock logic can programmed with Jumpers J1, J2, and J3 to produce interrupts at a 6Ø Hz or 3Ø Hz rate. The normal interrupt rate is 3Ø Hz (33.33 milliseconds). This normal rate is set by connecting J1 to J2.

Note: The screen print on the VDG Board has J1 labeled "14", J2 labeled "16, and J3 labeled "15".

This signal will end up at the Non-Maskable Interrupt input of the CPU. Upon receipt of this signal, the CPU will complete its current instruction cycle, then jump to address ØØ66H. This address contains a pointer to the Real Time Clock Interrupt Service routine.

RTC INT (TP 23) — From Pin 9 of U16. There is nothing on the schematic to indicate that this signal is used.

RTC* — From 13 of U14. To Pin 47 of the Model II System Bus.

Note: This signal is also shown on sheet 3 of the CPU schematic. It is labeled "RTC, SH.2" at Pin 47 of the Model II System Bus. There is no indication that this signal is used on the CPU Board.

FERD* — From Pin 11 of U31.

This signal is used at Pin 13 of U16 to clear signal "NMIRQ*" (see same) of the Real Time Clock circuit.

BLNKVID* — From Pin 14 of U18. This signal is controlled through software by writing to Port FF with Data Bit 6 set to a logic high. This signal will blank the entire display screen when it is asserted.

This signal is applied to Pin 8 of U38 to become one of the four Status signals which is polled by the CPU when it does a Read to Port FF.

Signal "BLNKVID*" is also applied to Pin 5 of U15/1 where it is used to block signal "DISPEN" (see same). A blocked "DISPEN" signal will blank the entire display screen.

ENABLE RTC INT*

From Pin 3 of U18. This signal is controlled through software by writing to Port FF with Data Bit 5 set to a logic high.

To Pin 2 of U38 to become one of the four Status signals which is polled by the CPU when it does a Read to Port FF.

ENABLE RTC INT

From Pin 2 of U18. This signal is the inverse of signal "ENABLE RTC INT*". It is used at Pin 13 of U29 to enable the Real Time Clock logic.

8Ø*/4Ø CHAR EN*

From Pin 6 of U18. This signal is controlled through software by writing to Port FF with Data Bit 4 set to a logic high.

To Pin 4 of U38 to become one of the four Status signals which is polled by the CPU when it does a Read to Port FF.

8Ø*/4Ø CHAR EN

From Pin 7 of U18. This signal is the inverse of signal "8Ø*/4Ø CHAR EN*". It is used at Pins 1, 2, and 13 of U28/1 to set the Character Display format of the screen. The screen will be in the 4Ø-Character Display mode when this signal is at a logic high.

FFRD* (TP 25) From Pin 12 of U31. This signal is applied to Pin 1 of U38. It is generated as necessary by TRSDOS® to read the following Status signals.

D7 Keyboard Interrupt Request.

A logic high indicates that the Keyboard is in the process of requesting an interrupt.

D6 Video Display Enable.

A logic high indicates that the video signals to the display screen are blocked.

D5 RTC Interrupt Enable.

A logic high indicates that the Real Time Clock circuit is enabled.

D4 Video Character Mode.

A logic high indicates that the the format of the video Display is set to the 4Ø-Character Mode.

FFWR* (TP 25) (TP 1Ø) From Pin 12 of U31. To Pin 9 of U18.

A Write to this port is used as follows.

D7 VDG Enable.

A logic high will enable the VDG circuit for a subsequent CPU access of the video RAMs.

D6 Video Display Enable.

A logic high will disable, or blank the video Display.

D5 Real Time Clock.

A logic high will enable the Real Time Clock.

D4 Video Display Mode.

A logic high will enable the 4Ø-Character Display Mode.

The data bits of the lower nibble are used in the Bank Select circuit of the Memory Board.

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VDG Board Port Allocation Table

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PORT ADDR.	READ FUNCTION	WRITE FUNCTION
FC	Read Keyboard data Clear Keyboard Interrupt	Load CRTC address Register
FD	Read CRTC Data Register	Load CRTC data Register
FE	Clear Real Time clock (RTC) interrupt	
FF	Read Non-maskable Interrupt Register and Non-maskable Interrupt Mask Register.	Load Memory Bank Select Register and load Non-maskable Interrupt Mask Register and Video enable.

VDG Board Test Points

TP 1	RCLOCK*	From Pin 8 of U1/1.
TP 2	VWR*	From Pin 6 of U2/2.
TP 3	DDISPEN	From Pin 1Ø of U12/1.
TP 4	CHSYNC	From Pin 6 of U5/1.
TP 5	HSYNC	From Pin 39 of U11/1.
TP 6	VSYNC	From Pin 4Ø of U11/1.
TP 7	DATA	From Pin 1 of J2. To Pin 1 of U6/2. This is the serial input data from the keyboard.
TP 8	FCRD*	From Pin 9 of U31/2.
TP 9	RCLOCKP	From Pin 12 of U1/1.
TP 1Ø	FFWR*	From Pin 8 of U3/2.

TP 11	CLOCK	From Pin 3 of J2. To Pin 8 of U6/2 and Pin 2 of U17/2. This is the clock signal from the keyboard. This test point is not labeled on the schematic.
TP 12	VOUT	From Pin 9 of U1Ø/1.
TP 13	MSP	From Pin 6 of U13/2.
TP 14	To Pin 11 of U15. To Pins 11 and 12 of U14. This terminal is labeled J1 on the schematic.	
TP 15	VSYNC	From Pin 4Ø of U11. This terminal is labeled J3 on the schematic.
TP 16	3Ø Hz	From Pin 5 of U16. This terminal is labeled J2 on the schematic.
TP 17	RCLOCKP*	From Pin 1Ø of U1/1.
TP 18	RCLOCK	From Pin 6 of U1/1.
TP 19	RCLOCKP	From Pin 12 of U1/1.

TP 2Ø	RCLOCK*	From Pin 8 of U1/1.

Note: The signals at TP 17, TP 18, TP 19, and TP 2Ø are used to adjust the CRT Display for clarity and sharpness. One of these test points must be jumpered to Pin 2 of U15/1. This is a "Trial-And-Error", or "Calibrated Eye-Ball" adjustment.

TP 21	IOBOE*	From Pin 3 of U2/2.
TP 22	IOBIE	From Pin 3 of U13/2.
TP 23	RTC INT	From Pin 9 of U16/2.
TP 24	VRD	From Pin 11 of U13/2.
TP 25	FFRD*	From Pin 12 of U31/2.
TP 26	CLOCK	From Pin 8 of U28/1.
TP 27	KBIRQ*	From Pin 5 of U17/2.
TP 28	MSEL*	From Pin 8 of U28/2.
TP 29	IOADSEL*	From Pin 8 of U27/2.

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Section Five

Model II Memory Board

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Contents

This glossary contains a list of working definitions on each of the control and handshake signals associated with the Memory circuitry.

Production Memory Boards are REV A and REV B. The Memory schematics reflect the circuits which are on the REV A Board. The differences between these Boards are minor.

Index for Memory Board Signals

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Glossary

Memory Board Control Line Signals

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SYNC* From Pin 18 of the Model II System Bus, from the CPU Board. This is the same signal as "M1*" generated by the CPU during the M1 or Op-Code Fetch cycle. It is used in the Pre-charge Extender circuit on the Memory Board to extend the pre-charge period of signal "RAS" at Pin 8 of U14 during an M1 cycle.

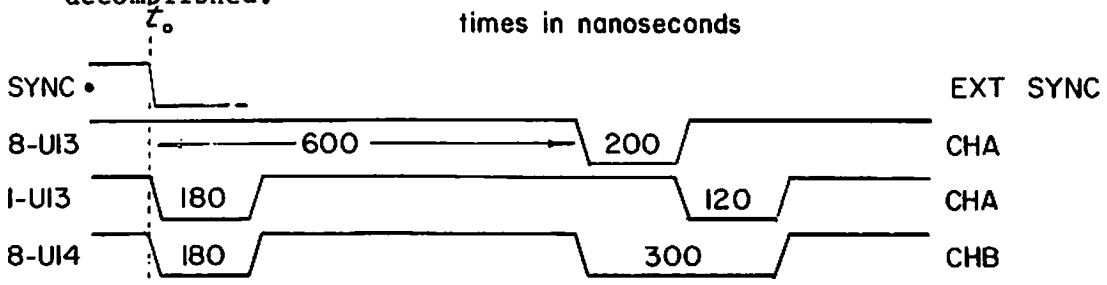
Understanding the Purpose of the Pre-charge Extender Circuit.

The pre-charge period is defined as the minimum time that "RAS*" must be negated before a next "RAS*" can be asserted: it is required so that data can be moved back from the RAMs' sense amplifiers into their appropriate bit cells after a Read or Write. For the 200 nanosecond RAMs used in the Model II, the minimum pre-charge period is specified as 120 nanoseconds.

With a 4 MHz System clock, the pre-charge period would become critical at T3 of an un-modified Op-Code Fetch cycle prior to refreshing memory, since the negated period of "RAS*" during this time would have a period of only 125 nanoseconds. Cutting pre-charge time too short would result in loss of data stored in RAM.

To eliminate this potential problem during the Op-Code Fetch cycle, a Wait state is introduced into each M1 cycle (See Section 1, CPU Board), extending "MREQ*", and signals "SYNC*" and "MEMCYC*" are used to extend pre-charge backwards to approximately 300 nanoseconds by negating RAS* before T3 time at Pin 8 of U14.

The measured timing diagrams below show how this is accomplished.



CLOCK — From Pin 44 of the Model II System Bus. Signal "CLOCK" is the 4 MHz System clock whose period is 25Ø nanoseconds.

MEMCYC* — From Pin 21 of the Model II System Bus. This is the same signal as signal "MREQ*" generated by the CPU during a Read or Write operation.

Signal "MEMCYC*" is used on the Memory Board to generate signal "RAS", and as an enable signal to the Data Buffer gate logic.

RD* — From Pin 9 of the Model II System Bus. To Pin 14 of Buffer U56 where it becomes signal "READ". This signal is used in the Data Buffer gate logic.

REFRSH* — From Pin 45 of the Model II System Bus. This signal is generated by the CPU during the T3 and T4 clock periods of the Op-Code Fetch cycle of an instruction.

"REFRSH*" is used on the Memory Board as a gate for "RAS*" during RAM refresh time. During this same time, "REFRSH*" asserted will also inhibit signals "CAS1*", "CAS2*", and "MUX" since these signals are not required for the refresh operation.

WR* — From Pin 2Ø of the Model II System Bus. This signal is generated by the CPU during the Memory Write cycle of an instruction. It is used on the Memory Board to create signals "WR1*", and "WR2*". This signal is also used in the Data Buffer gate logic.

IEIN — From Pin 13 of the Model II System Bus. To Pin 14 of the Model II System Bus. Pin 14 is tied to Pin 13 of the next card slot down the line.

IEOUT — From Pin 14 of the Model II System Bus. From Pin 13 of the previous card slot up the line.

Note: Signals "IEIN" and IEOUT" are loop signals of the daisy chain priority interrupt scheme.

BAKIN* — Pin 15 of the Model II System Bus. An output. To pin 16 of the next card slot down the line.

BAKOUT* — Pin 16 of the Model II System Bus. An input. From Pin 15 of the previous card slot up the line.

Note: "BAKIN*" and "BAKOUT*" are loop signals which form a daisy chain for multiple-DMA priority control. Not currently used in the Model II.

RESET* From Pin 67 of the Model II System Bus. This signal will be asserted during a Power-On or Manual Reset to clear the decoder U58 at Pin 1.

IOCYC* From Pin 22 of the Model II System Bus. This is the same signal as signal "IORQ*" of the CPU. It will be asserted during an Input/Output cycle of an I/O operation, and is used in creating "IOFFWR*" (see same).

"IOCYC*" will also be asserted during an Interrupt Acknowledge cycle of an instruction.

DISRO* From Pin 40 of the Model II System Bus. The only peripheral add-on device which currently uses this signal is the Communications Multiplexer unit, Stock Number 71-3000.

"DISRO*" is routed to U12 where it is designed to disable the RAM output of the Model II Memory Board when the MUX CPU Board in the Multiplexer is in the process of doing a ROM read. This signal will also be generated by the Quad UART Board in the Multiplexer.

Glossary

Memory Board On-Board Signals

IOFFWR* — From Pin 7 of U41. This signal will be asserted during a Write to Port FF. "IOFFWR*" is used as a clock at Pin 11 of Latch U58, which is used to latch the lower nibble of the data byte onto the Memory Board to select 1 of 15 possible Memory Pages.

Data Bit "D7" is also latched by U58. This bit is used to enable or disable Page 1 of Bank Ø since the addresses of the last 2K of the System Address Space is also shared with the Video RAMs. The Memory Board will be disabled in this address range when "D7" is a logic high - indicating that the CPU is in the process of accessing the Video RAMs.

"IOFFWR*" is also used in the Data Buffer gate logic at Pin 13 of U26 to generate signal "SELECT*" (see same).

SELECT* — To Pin 43 of the Model II System Bus. This signal will be asserted during a Write to Port FF, or during a Memory Read/Write operation. There is no indication that this signal is used at any time.

RAS — From Pin 8 of U14. This signal is derived from signal "MEMCYC*" (see same) in any RAM Read and during the refresh period of an Op-Code Fetch cycle. During the refresh time, "RAS" is modified by U13 to extend the pre-charge period (see discussion, Page 5-3).

CAS*
CAS1*
CAS2* — To Pin 15 of the RAMs. Signals "CAS1*" and "CAS2*" will become asserted approximately 6Ø nanoseconds after "RAS*" is asserted. The delay is generated by U42, a tapped delay line IC.

Signal "CAS*" is the Column Address Strobe for the RAMs. It is also used as a Chip Enable signal.

The RAM access time specification is based on the moment "CAS*" is asserted during a Memory Read instruction cycle. For the 2ØØ nanosecond RAMs used on the Memory Board, this specification is a guarantee that the data on the Bus will be stable 135 nanoseconds after "CAS*" is asserted.

MUX — From Pin 1Ø of U28. To Pin 1 of Multiplexers U39 and U4Ø. "MUX" is used to convert the System addresses of the CPU into the Row and Column addresses for the RAMs during a Read or Write operaton.

"MUX" is normally at a logic low. During this time, the Row address will be latched into the RAMs on the falling-edge of "RAS*". Approximately 2Ø nanoseconds later, "MUX" will switch to a logic high; and after an additional delay of 4Ø nanoseconds, "CAS*" will be asserted and latch the Column address into the RAMs.

BS* — A programmable signal out of the Three-to-Eight Decoder U43. "BS*" can be programmed to represent 1 of 8 banks of Memory Boards. Once programmed, it is used as a Memory Board enable signal at Pin 6 of U11.

BANK* — From Pin 8 of U1Ø. To Pin 1 of U29. "BANK*" is a conditional output signal from the Memory Disable circuit illustrated on page 5-12. It is used on the Memory Board to enable/disable Pages 1-15 of the System Address Space. This "Space" can be disabled under the following conditions.

* When "BS*" is negated.

  This condition indicates that the Memory Board is not selected (Base Page is always enabled).

* When Address line A15 is at a logic low.

  This condition indicates that the upper page of the System Address Space is not being accessed.

* When Address lines AD11, AD12, AD13, and AD14 are at a logic high, along with Data Bit 7.

  This condition will be true starting at address F8ØØH to indicate that the CPU is in the process of accessing the video RAMs.

MSEL — From Pin 6 of U26. This signal will be asserted when the CPU is in the process of doing an Op-Code Fetch, or a Memory Read/Write. To Pin 4 of U14 where it is ANDed with signal "MEMCYC" to enable the Read/Write gates of the Data Buffer gate logic.

RAS* To Pin 4 of the RAMs. From the NAND gates, U24. "RAS*" is the Row Address Strobe signal for the RAMs.

During a Read or Write operation, "REFSH*" is negated high at the NOR gates, U25, but only one of the Row Select Lines from U29 is low: only one output line from U25 will be high for the 16K RAM Row selected. This high is NANDed with "RAS" at the appropriate gate of U24 to produce "RAS*" asserted, thus causing the Row address to be latched into only the selected RAM Row. According to the RAM specifications, "RAS*" must remain at a logic low for a minimum period of 200 nanoseconds during either a Read or a Write.

During the T3 and T4 times of the M1 cycle, the Z80A is decoding and executing an Op-Code, and is not using any of the Control, Address or Data Buses. Refresh occurs during this period of time, and is thus "transparent" to the user.

On assertion of the "REFRSH*" signal at T3 time of the M1 cycle, all output lines from the NOR gates, U25, will be high regardless of the state of the select lines from U29, and a Row address will have been put on the lower 7 bits of the Address Bus from the Z80A's Refresh Counter Register. Now assertion of "RAS*" will strobe into the RAM the refresh row address for the internal RAM row, initiating the internal sequence of refresh for all RAM (including those of any other Pages) simultaneously. "MUX" and "CAS*" are not generated during this time. The RAM bit cells in the internal row addresses are destructively transferred to the internal sense amplifiers. When "RAS*" is then negated, the information in the sense amplifiers is written back to the bit cells in the appropriate row, thus accomplishing a refresh of those bit cells. See the discussion on negation and assertion of "RAS" on Page 5-3 relative to Pre-charge before memory refresh. See the Z80 Technical Manual and RAM Data Specification Sheets for additional detail.

Page and Bank Definitions

There is no standard industry definition for the words "PAGE" and "BANK" as applied to Memory Systems. The terms seem to be used interchangeably by the industry.

To eliminate any confusion, the definitions of the words "PAGE" and "BANK" as applied to the Model II/12/16 are outlined below.

The Z8Ø processor used in these computers has 16 address lines, allowing the addressing of 65,536 (64K) bytes of Memory. This is known as the ABSOLUTE ADDRESS SPACE, as the Z8Ø can address any one of the 64K bytes without extra hardware or software.

With special hardware and software, the Z8Ø can be made to access up to 512K of Memory, limited only by available motherboard slots, power supply and software. This additional Memory is known as LOGICAL MEMORY, made up of groups of ICs called PHYSICAL MEMORY.

In the case of the stock Model II, the ABSOLUTE, LOGICAL and PHYSICAL Memory are all the same thing. Definition problems arise, however, with any Memory expansion (e.g., an additional 64K Board for Enhanced Visicalc), or with addition of peripheral devices which also contain memory accessed by the Z8Ø (e.g., Hard Drives).

In the Model II/12/16 computers, the term "BANK" is defined as:

"BANK - A block of 65,536 contiguous bytes of RAM."

The implication is that a Bank of Memory is completely contained in one set of Memory ICs. In the stock Model II, the 64K Memory Board is itself one Bank of Memory. However, the 144K Memory Board can contain up to two full Banks of Memory and part of a third, each Bank consisting of eight 64K RAM ICs, and the partial Bank consisting of eight 16K RAM ICs.

Thus, "MEMORY BANK", "MEMORY BOARD", and "MEMORY CARD" are not necessarily synomymous. The 64K Board IS one Bank, but the 144K Board is addressed as three Banks.

Each Physical Bank of Memory consists of two Physical Pages of Memory. In the Model II/12/16 computers, the term "PAGE" means:

"PAGE - one-half of a Memory Bank, 32,768 contiguous bytes of Memory.

Therefore, each Memory Bank contains two Memory Pages, Page Ø and Page 1. Each Physical Bank can be designated as any Logical Bank with push-on jumpers. Thus, it is not necessary to purchase a special "Bank Ø" or "Bank 1" Memory Board, as any Memory Bank on any Memory Board may be designated to become any Logical Bank.

Remember, however, that the Z8Ø can address only an ABSOLUTE Memory Space of 64K bytes. The special hardware and software mentioned above allow the computer to switch portions of LOGICAL Memory into or out of the Z8Ø's ABSOLUTE Memory Space. This technique is called PAGE SWITCHING, by virtue of which the Z8Ø still addresses only 64K Memory bytes at any one time, but Pages of LOGICAL Memory are switched in or out of ABSOLUTE Space as needed.

The hardware to control Page Switching is addressed at Port FF. The low-order Data Nibble is decoded to control switching of the LOGICAL BANK and LOGICAL PAGE in or out of the ABSOLUTE Address Space as follows:

Port FF	Data Bit Ø:	Page Select (Ø or 1)
	Data Bit 1:	
	Data Bit 2:	Bank Select (Ø to 7)
	Data Bit 3:	

Data Bits 1-3 permit selecting any one of eight Banks. Data Bit Ø permits selecting either of two Pages, Ø or 1, within a Bank. Thus the Bank/Page Select circuitry permits selecting up to 16 LOGICAL PAGES numbered from ØH (Bank Ø Page Ø) to FH (Bank 7 Page 1).

Logical Page Ø (Bank Ø Page Ø) is special. This Page is NEVER switched out of the System using bank-switching techniques. It is ALWAYS found at Memory location ØØØØH to 7FFFH in the Z8Ø ABSOLUTE Memory Space. Because of this it is also referred to the the BASE PAGE. Whatever operating system (such as TRSDOS®) the computer is running resides in BASE Page, along with Interrupt, Restart and Reset vectors, and many supervisor routines: without being able to access the operating system or these vectors and routines, the Z8Ø would be unable to perform its functions. Thus, BASE Page is NEVER switched out of the System.

The remaining 15 LOGICAL Pages (1H to FH) are selected with the low-order Port FF Data Nibble mentioned above, and the Page selected now becomes address range 8ØØØH to FFFFH, or the upper 32K of Memory, in the Z8Ø's ABSOLUTE Address Space.

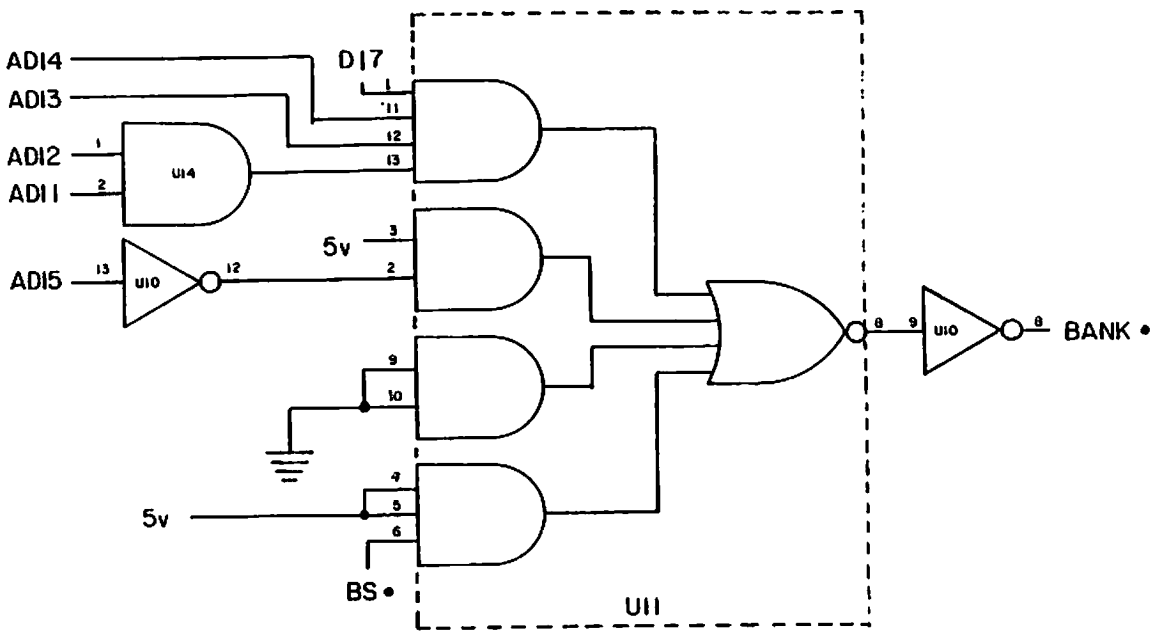
Since BASE Page (LOGICAL Page Ø) is never switched out, a program utilizing more than 64K of LOGICAL Memory must use this Memory one 32K Page at a time. For example, Enhanced Visicalc uses a total of 128K of Memory. BASE Page is fixed, containing not only the operating system but also much of the Visicalc program. The software uses LOGICAL Pages 1-3 for data manipulation and storage.

By properly programming Port FF, the Visicalc program selects which one of the three LOGICAL Pages it needs to use as the upper half (8ØØØH to FFFFH) of the Z8Ø's ABSOLUTE Address Space.

As an example, suppose Visicalc needs to use LOGICAL Page 3, which is physically Bank 1 Page 1. Visicalc must set the low-order Data Nibble of Port FF to 5 (binary ØØ11). Data Bit Ø selects Physical Page 1, and Data Bits 1-3 select Physical Bank 1. This Page now become the upper half of the Z8Ø's ABSOLUTE Address Space, and will be accessed by the Z8Ø in a normal manner. Note, while LOGICAL Page 3 is switched in, LOGICAL Pages 1 and 2 (which are Bank Ø Page 1 and Bank 1 Page Ø) are switched out.

It is possible to construct Memory such that any given LOGICAL Page does not contain a full 32K of Memory. Examples of this are the Hard Drive Interface Boards and ARCNET, each of which require only 16K, or one-half a LOGICAL Page, of additional Memory.

Note that even though only two LOGICAL Pages will be available to the Z8Ø at one time during Op-Code Fetches or Memory Read/Write operations, ALL Memory Pages are refreshed simultaneously during the refresh period of the M1 cycle (see discussion on Pre-charge Extender circuitry, page 5-3). Refresh does not involve a Read or a Write, so that no Memory address contention between Physical Pages occurs. Thus, all Memory in all Pages is refreshed "in parallel" so that data on all Pages, switched in or not, is not lost.



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