# CPU BOARD

## FUNCTIONAL SPECIFICATIONS

The TRS-80 Communications Multiplexer CPU Board provides for the system the following functions:

1. Performs data processing activities.
   a) Supports mode 2 vectored interrupts.
2. Provides dual serial I/O channels.
   a) RS-232C standard signals.
   b) Asynchronous and synchronous schemes supported.
      Bisync, SDLC, and HDLC protocols are supported.
3. Provides timing signals needed by the system.
   a) 2 or 4 MHz system clock option.
   b) Programmable serial I/O baud rate clocks.
   c) Real time clock.
   d) Control signals for system boards
   e) Flexible on or off board wait state generation.
4. System bootstrap firmware (2716 compatible).
5. Power on and manual reset logic.

Major components of the CPU Board are:

Z-80A CPU chip (Central Processing Unit)

Z-80A SIO chip (Serial Input/Output)

Z-80A CTC chip (Counter Timing Circuit)

2716 Compatible ROM (Read Only Memory)

## THEORY OF OPERATION

### Decoding Logic

The peripheral devices on the CPU Board are I/O mapped with the exception of the BOOT ROM. The port addresses used are F0H through F9H. Port mapped devices use only the lower eight address bits to specify which port is being addressed. The upper eight address bits are ignored completely; they are not relevant to port mapped devices. Three other signals (WR*, RD*, and IOCYC*) are used by port mapped devices to determine whether an input or output operation is occurring. An input operation is in progress if IOCYC* and RD* are both low. An output operation to the addressed port is in progress if IOCYC* and WR* are both low.

The upper left part of Sheet 3 of the CPU schematic should now be referred to. U38, U37, and one half of U24 are used to decode the I/O addresses required for the CPU Board. U38 is an open-collector output BCD to decimal decoder which, depending upon the binary combination presented to inputs A through D, brings one of its outputs low. These outputs become the chip enables for the peripheral devices used.

One half of U37 is used to detect when any of the ports are being addressed. Its output is inverted and presented to pin 4 of U24. One half of U26 and one fourth of U25 detect an input or output operation in progress, based on the state of RD*, WR*, and IORQ*. This output is presented to pin 5 of U24. A low is produced at pin 6 of U24 when any of the valid ports are addressed and an input or output operation is in progress. This low signal goes to pin 9 of U25 and is combined with the signal RDROM* at pin 10 of U25. This combination produces a low-going strobe labeled SELECT* at pin 8.

RDROM* goes low if a Read from the BOOT ROM is in progress; therefore, if SELECT* is low, either an input/output operation to the valid ports is ocurring or a Read from the BOOT ROM is occurring. SELECT* is gated to pin 43 of the system bus via a tri-state buffer (one fourth of U39). This signal may be monitored with an oscilloscope (to verify proper operation of the decoding logic) while executing a diagnostic program.

The BOOT ROM (a 2716 EPROM or a compatible mask ROM) is a memory mapped device which, when enabled, occupies the lower 4K of the system address space (0000H to 0FFFH). Three fourths of U17 decodes the upper address bits (A12 to A15) to detect an address within this range. The output produced from this logic (U17 pin 8) is gated with ROM*/RAM* (if the BOOT ROM is enabled) to produce a low at pin 11 of U17. U19 combines this signal with the output of A11 and its logical inverse to produce two ROM chip enables: ROM0CE* and ROM1CE*.

ROM0CE* is active for the address range 0000H to 07FFH. ROM1CE* is currently not used. RD* and MREQ* are decoded by one fourth of U26 to detect a memory read in progress. When this signal (pin 11 of U26 and ROM0CE*) is low, the BOOT ROM is allowed to gate out the data pattern corresponding to the byte being addressed, to the internal data bus.

IORQP* and WR* are decoded by one fourth of U26 to produce the signal labeled OUT* (U26 pin 8). This output, when combined with the signal F9* (U38 pin 11), produces a low-going strobe at pin 3 of U24. This signal indicates that an output operation is occurring to port F9H. The rising edge of this signal latches the state of D0 into U23. The Q* output of flip-flop U23 is fed back to pin 13 of U17 and enables or disables the BOOT ROM. If D0 is reset the BOOT ROM will be disabled. The set input of this flip-flop is tied to RESET*; therefore, power on or manual Reset will automatically enable the BOOT ROM. Below is a table which outlines the port address allocations for the CPU Board.

**PORT ADDRESS ALLOCATION**

| Port No. | Allocation | Function |
|---|---|---|
| F0H | CTC | Channel 0 |
| F1H | CTC | Channel 1 |
| F2H | CTC | Channel 2 |
| F3H | CTC | Channel 3 |
| F4H | SIO A | Channel A data |
| F5H | SIO B | Channel B data |
| F6H | SIO A | Channel A Command/Status |
| F7H | SIO B | Channel B Command/Status |
| F8H | DMA | DMA Command/Status |
| F9H | ROM ENABLE LATCH | ENABLES/DISABLES ROM |

Bus Steering Logic

The system data bus is a bidirectional path, that is, data may be driven to, or received from, the system bus. Outputs to external ports or Writes to the system memory require that data be driven to the system bus. Inputs from external ports, interrupt acknowledges from internal devices, or Reads from system memory other than the BOOT ROM require that the data is received from the system bus. This problem is somewhat complicated by the fact that data must not be received from the system bus when an input, interrupt acknowledge from an external device, or a Read operation from CPU Board resident devices is in progress.

Data is switched to and from the sytem bus by U32 and U33. One third of U40 is used to detect a READ, an interrupt acknowledge, or an input cycle in progress. Pin 12 of U40 goes low if any of these operations occur.

One half of U11 and one fourth of U28 detect the presence of a pending interrupt from a device on the CPU Board. An interrupt request from a device on the CPU Board will force pin 10 of U11 low, which in turn forces pin 8 of U11 low. This output is combined with INTAK* at pins 1 and 2 of U28 to produce the signal LOCAL INT PENDING. When this signal goes low, U40 pin 4 is prevented from going low. This action indicates that an interrupt acknowledge from one of the CPU Board devices is in progress and that the data bus receivers should not be enabled.

SELECT* (U40 pin 5) performs the same function if any of the devices on the CPU Board are selected by a memory read or an I/O operation. When pin 3 of U40 is high it will force pin 6 of U40 low provided that pin 4 and 5 of U40 are both high. This enables the data receivers to gate data onto the CPU data bus for a memory read, an input operation, or an interrupt acknowledge.

Manual and Power On Reset Logic

If the RESET* input on the CPU chip goes low during T3 of an M1* cycle, approximately ten T states later the MREQ* will go to an indeterminate state for one T state. This action could cause an aborted or short access of the dynamic RAM which will cause destruction of data present in the RAM. To avoid this problem, the falling edge of the RESET input must be synchronized with the falling edge of M1*. One half of U11 and one half of U12 perform this synchronization as well as provide a one-shot to limit the duration of the CPU RESET pulse. The one-shot duration is approximately 50 useconds per switch depresion. This duration is required to avoid suspending CPU refresh of Dynamic RAM which could destroy memory contents. The connector, J2, connects the reset switch to this logic and also provides the +5 volts for the front panel indicator lamps.

System Clock Generation Circuit

The heart of the clock generation logic is an 8 MHz crystal oscillator formed by Y1, C21, R20, R21, and three 'LS74 flip-flops (see sheet 1 of the schematic). The output, U31 pin 8, is an 8 MHz square wave. This signal is divided down by U23 and U30 to produce 4 MHz, 2 MHz, and 1 MHz clocks as needed by the system. The 8 MHz signal is buffered by U13 and fed directly to pin 46 of the system bus. A jumper option is provided to select either a 4 MHz or a 2 MHz main system clock for the Z-80 family parts. This output is divided by 2 and is then sent as clock inputs for the Z-80 CTC when operating in the counter mode. Normal system operation requires the main system clock to run at 4 MHz.

The output of U31 pin 8 (main system clock) is conditioned by the clock buffer circuitry consisting of Q1, C16, R13, R14, R15, and a 74S04 inverter. The clock buffer circuitry ensures fast rise and fall times and close to 5 volts peak-to-peak amplitude transitions. These clock characteristics are important to the Z-80A family of components when operating at maximum frequency (4 MHz).

Wait State Generation Logic

The memory access time requirements are most severe during an M1 cycle instruction fetch. All other memory accesses have an additional one half clock cycle to be completed. The TRS-80 Multiplexer system uses 200 nsecond access time RAMS. One wait state must be inserted on M1 cycle instruction fetches when using this speed of memory. The BOOT ROM is, at best, a 300 nsecond access time

device which requires one wait state per memory access, if the BOOT ROM is enabled. U29 along with some associated gating, provides the wait state generation. This feature is provided for external system boards which require non-standard timing for one reason or another.

Interrupt Priority Logic

The Z-80 interrupt structure allows up to four Z-80 family parts to be connected in a daisy chain fashion without any additional logic. Interrupt priority of a device is set by that device's location on the daisy chain. the highest priority is given to the CTC chip which has its IEI (Interrupt Enable In) line tied high to +5 volts. The next priority device is the SIO whose IEI line is tied to the CTC's IEO (Interrupt Enable Out). This scheme works fine unless more than four interrupting devices are connected to the daisy chain. The Mulitplexer system has more interrupting devices; therefore, more logic is needed in the Multiplexer CPU system than is used in the standard TRS-80 Model II CPU system.

The INT* line is sampled at the beginning of the last T state of the last M1 cycle of an instruction. Upon acceptance (if IFFI=1 and interrupts are enabled) an interrupt acknowledge will be performed. This consists of a special M1* cycle with an IORQ* signal instead of the normal MREQ*. At the leading edge of M1* and before the leading edge of IORQ*, peripherals are free to contend for service. The CPU will automatically insert one more wait state to allow for additional ripple time for priority determination.

The presence of extra I/O devices in the Multiplexer system calls for extending the interrupt acknowledge cycle time. The technique employed here (see sheet 2 of the schematic) involves gating the IORQ* line to the peripheral devices. When M1* goes low without an active RD* (indicating an active interrupt acknowledge sequence), the WAIT* line is activated and IORQP* to the peripherals is maintained high until a time-out on a LS161 counter (U1) occurs. The length of this time-out is determined by the setting of a four-position DIP switch, S1. For standard operation, S1 is set as follows:

| | |
|---|---|
| positions 1, 3, and 4 | OFF |
| position 2 | ON |

This gives a generated wait of 2 useconds. Another valid situation for an interrupt acknowledge sequence occurs when IORQ* and M1* both go low.

EIA Buffers

The logic internal to the CPU Board (SIO inputs and outputs) operate with TTL logic levels (3.5V or greater = Logic 1; 0.8V or less = Logic 0). EIA logic levels (-3V or less = Logic 1; +3V or greater = Logic 0) are used for interfacing two RS-232C devices. The logic levels must therefore be converted from one convention to the other when interfacing to external devices. U4, U6, and U8 provide the EIA to TTL conversion while U5 and U7 provide the TTL to EIA conversion.

CTC Operation

The CTC (Couter Timing Circuit), U14, is used to generate clocks for the SIO Receive and Transmit on Channels A and B. The CTC also provides a real-time clock for interrupts. CTC output Z/C/T0 (pin 7 of U14) is connected to pins 13 and 14 of U15 (SIO) via jumper option G-H. This connection provides Channel A Receive and Transmit clocks.

CTC output Z/C/T1 (pin 8 of U14) is connected via jumper option Q-R to pin 27 of U15 (SIO). This connection provides Receive and Transmit clcks for Channel B. CTC output Z/C/T2 (pin 9 of U14) is connected via jumper option B-C to pin 20 of U14 (CTC CLK/TRG3) and provides real-time clocking. Pins 21, 22, and 23 of U14 are tied to the 2 MHz clock output, U30 pin 5.

Jumper Options

The Multiplexer CPU board has several user selectable jumper options. Below is a list of the standard jumper positons and a brief description of each.

| | |
|---|---|
| A-B-C | This option is standard in position B-C which uses the CTC to provide real-time clocking. |
| D-E-F | This option is normally set E-F and in- |

volves generating the WAIT* logic by determining a valid interrupt acknowledge sequence.

G-H-J — This option must be set to G-H to provide SIO channel A with receive and transmit clocks.

K-L-M-N — This option is used to provide independent receive and transmit clocks for SIO channel A. Standard Multiplexer operation cannot use this option and it should be left open.

P-Q-R — This option provides the receive-transmit clocks for SIO Channel B and should be set on Q-R.

S-T-U — This should be set on S-U to enable OPCODE waits (when the ROM is latched in).

V-W-X — This is the 2/4 MHz clock option and is set to W-X for normal 4 MHz operation.

Y-Z-AA — This is the 4/8 MHz precompensation option and is set to Z-AA to provide the system bus with an 8 MHz clock.

# CPU PARTS LIST

| SYMBOL | DESCRIPTION | MAN. PART # | R.S. PART # |
|---|---|---|---|
| | **Capacitors** | | |
| C1 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C5 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C6 | | | |
| C7 | 100uF, 16V, elect, axial | 8317101 | ACC107QDAA |
| C8 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C9 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C10 | 1000pF, 50V, cer. disc | 8302104 | ACC102QJCP |
| C11 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C15 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C16 | 33pF, 50V, cer. disc | 8300334 | ACC330QJCP |
| C17 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C20 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C21 | 470pF, 50V, cer. disc | 8301474 | ACC471QJCP |
| C22 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C26 | 0.1uF, 50V, mono, axial | 8374104 | ACC104QJCA |
| C27 | 100uF, 16V, elect, axial | 8317101 | ACC107QDAA |
| C30 | 100uF, 16V, elect, axial | 8317101 | ACC107QDAA |
| | **Crystal** | | |

| | | | |
|---|---|---|---|
| Y1 | 8 MHz | 8409006 | AMX2571 |
| | **Connector** | | |
| J2 | Header, 4 position | 8519053 | AJ6791 |
| | **Diode** | | |
| CR1 | 1N4148 | 8150148 | ADX1152 |
| | **Integrated Circuits** | | |
| U1 | 74LS161A, 4-bit counter | 8020161 | |
| U2 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U3 | 74LS10, triple 3-in NAND | 8020010 | AMX3898 |
| U4 | SN71489, quad line receiver | 9050189 | |
| U5 | SN71488, quad line driver | 9050188 | |
| U6 | SN71489, quad line receiver | 9050189 | |
| U7 | SN71488, quad line driver | 9050188 | |
| U8 | SN71489, quad line receiver | 9050189 | |
| U9 | TMS2716, EPROM | 8042716 | |
| U10 | 74LS132, quad 2-in NAND | 8020132 | AMX3561 |
| U11 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U12 | 74121, one-shot | 8000121 | |
| U13 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U14 | Z-80A, CTC | 8047882 | AXX3016 |
| U15 | Z-80A, SIO | 8047884 | AMX3018 |
| U16 | Z-80A, CPU | 8047880 | AXX3014 |
| U17 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U18 | 74LS04, hex inverter | 8020004 | AMX3552 |
| U19 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U20 | 74LS125, quad 3-state buffer | 8020125 | AMX4640 |
| U21 | 74LS04, hex inverter | 8020004 | AMX3552 |

| | | | |
|---|---|---|---|
| U22 | 74LS08, quad 2-in AND | 8020008 | AMX3698 |
| U23 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U24 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U25 | 74LS08, quad 2-in AND | 8020008 | AMX3698 |
| U26 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U27 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U28 | 74LS32, quad 2-in OR | 8020032 | AMX3557 |
| U29 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U30 | 74LS74, dual D flip-flop | 8020074 | AMX3558 |
| U31 | 74S04, hex inverter | 8010004 | |
| U32 | 8T26A, bus transceiver | 8060026 | AMX4261 |
| U33 | 8T26A, bus transceiver | 8060026 | AMX4261 |
| U34 | 74LS244,octal 3-state buffer | 8020244 | AMX3864 |
| U35 | 74LS240,octal3-stateinverter | 8020240 | AMX4225 |
| U36 | 74LS240,octal3-stateinverter | 8020240 | AMX4225 |
| U37 | 74LS20, dual 4-in NAND | 8020020 | AMX3555 |
| U38 | 74LS145, 1-of-10 decoder | 8020145 | |
| U39 | 74LS125, quad 3-state buffer | 8020125 | AMX4640 |
| U40 | 74LS10, triple 3-in NAND | 8020010 | AMX3898 |
| | Resistors | | |
| R1 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R2 | 4.7K, 5-pin SIP resistor pak | | |
| R3 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R4 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R5 | 10K, 1/4W, 5% | 8207310 | AN0281EEC |
| R6 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R7 | 10K, 1/4W, 5% | 8207310 | AN0281EEC |

| | | | |
|---|---|---|---|
| R8 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R9 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R10 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R11 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R12 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R13 | 1.2K, 1/4W, 5% | 8207212 | AN0199EEC |
| R14 | 220 ohm, 1/4W, 5% | 8207122 | AN0149EEC |
| R15 | 22 ohm, 1/4W, 5% | 8207022 | AN0078EEC |
| R16 | 4.7K, 1/4W, 5% | 8207247 | AN0247EEC |
| R17 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R18 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R19 | 2.2K, 1/4W, 5% | 8207222 | AN0216EEC |
| R20 | 910 ohm, 1/4W, 5% | 8207191 | AN0192EEC |
| R21 | 910 ohm, 1/4W, 5% | 8207191 | AN0192EEC |
| R22 | 2.2K, 5-pin SIP resistor pak | | |

Transistor

| | | | |
|---|---|---|---|
| Q1 | 2N3906 | 8100906 | AMX3584 |

MISCELLANOUS

| Description | Quanity | Man. Part# | R.S. Part# |
|---|---|---|---|
| Jumper Plug | 7 | 8519021 | AJ6769 |
| Socket, 8-pin | 1 | 8509011 | |
| Socket, 14-pin | 29 | 8509008 | AJ6759 |
| Socket, 16-pin | 4 | 8509003 | AJ6581 |
| Socket, 20-pin | 3 | 8509009 | AJ6760 |
| Socket, 24-pin | 1 | 8509001 | AJ6579 |

| | | | |
|---|---|---|---|
| Socket, 28-pin | 1 | 8509007 | AJ6758 |
| Socket, 40-pin | 2 | 8509002 | AJ6580 |
| Staking Pins | 20 | 8529014 | AHB9682 |