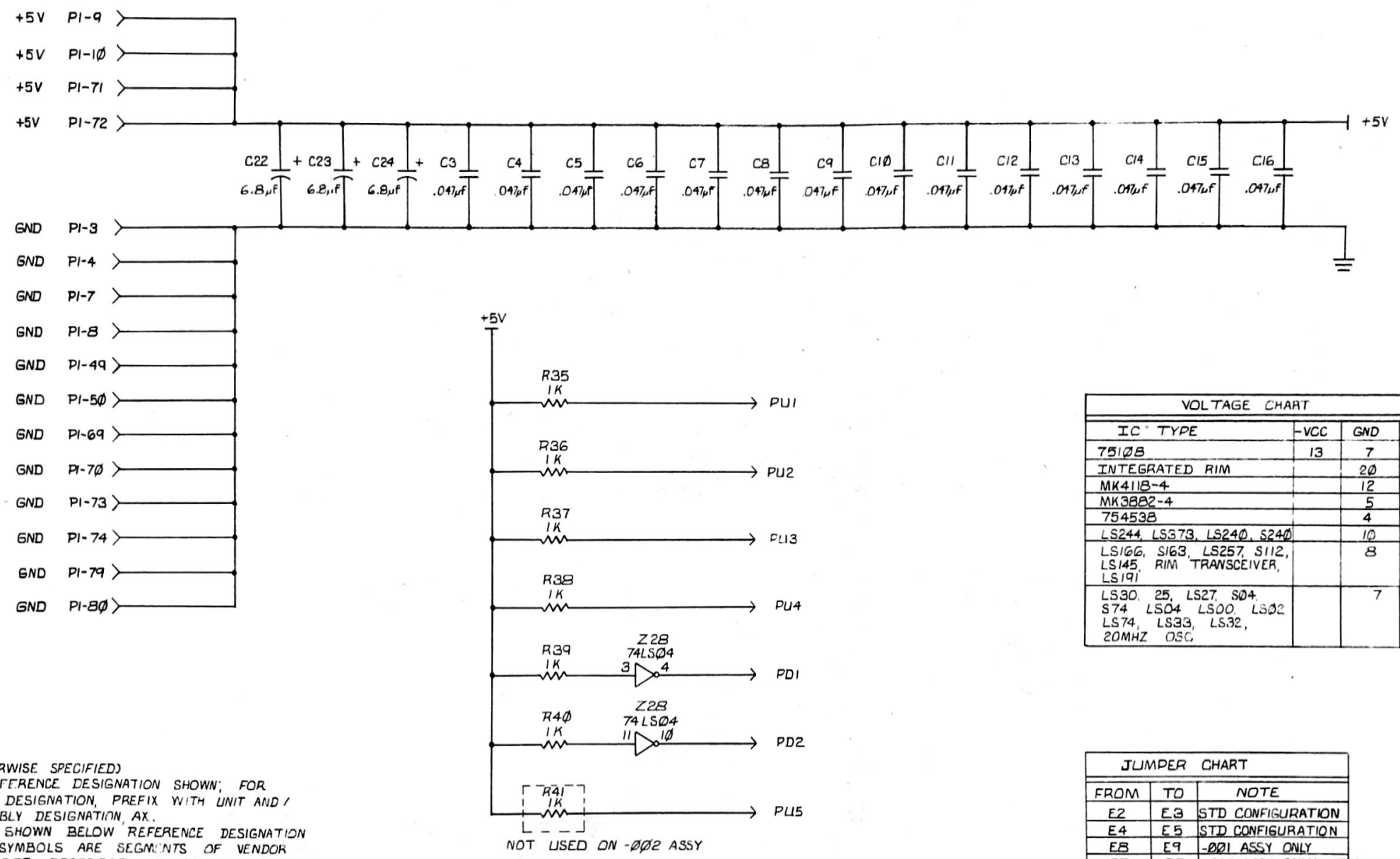




NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. PARTIAL REFERENCE DESIGNATION SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND / OR ASSEMBLY DESIGNATION, AX.
2. NUMBERS SHOWN BELOW REFERENCE DESIGNATION IN LOGIC SYMBOLS ARE SEGMENTS OF VENDOR PART NUMBER DESCRIBED IN PART. LIST
3. LOGIC SYMBOLS PER USA-STD Y32.14; ELECTRONIC SYMBOLS PER USA-STD Y32.2-67
4. ALL RESISTOR VALUES ARE IN OHMS, 5% 1/4 W

VOLTAGE CHART			
IC TYPE	-VCC	GND	+5V
7510B	13	7	14
INTEGRATED RIM		20	39
MK411B-4		12	24
MK38B2-4		5	24
75453B		4	8
LS244, LS373, LS240, S240		10	20
LS100, S163, LS257, S112, LS145, RIM TRANSCEIVER, LS191		8	16
LS30, 25, LS27, S04, S74 LS04, LS00, LS02, LS74, LS33, LS32, 20MHZ OSC		7	14

REF DES	
LAST USED	NOT USED
T1	
J2	
R46	R32, R33
CR1	
C32	
Z49	
L5	
Q3	
F9	

JUMPER CHART		
FROM	TO	NOTE
E2	E3	STD CONFIGURATION
E4	E5	STD CONFIGURATION
E8	E9	-001 ASSY ONLY
E7	E8	-002 ASSY ONLY

SPARES			
REF DES	TYPE	INPUT	OUTPUT
Z6	LS33	11, 12	13
Z20	S04	11	10
Z31	LS00	13, 12	11
Z31	LS00	9, 10	8
Z31	LS00	4, 5	6
Z13	7425	9, 10, 12, 13	8

MATERIAL	UNLESS OTHERWISE SPECIFIED	DRAFTMAN: JLS, BOYER, TERRY	DATE: 12-6-82	REF: DRILL PLAN 1700216
FINISH	TOLERANCES	CHECK	DATE	SCHEMATIC DIAGRAM ARC INTERFACE BOARD
	XX = ± .010 XXX = ± .005	DESIGN	DATE	
	ANGLES = 21°	APPD	DATE	
	HOLE DIA TOLERANCES	APPD	DATE	
	.014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001			
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING			
	DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON	
DWG. NO. 8000178				SIZE
SCALE NONE				SHEET 1 OF 4

