even address upper byte
odd address low byte

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

built for odd parity.

inbound data buffers

outbound data buffers

parity checkers

COMPONENT SIDE

J2 J0 J1

20000-3FFFF 6000-7FFF

0-1FFFF 4000-5FFF

R/W UPPER BYTE CAS0

R/W LOWER BYTE CAS1

RAS0 U

RAS1 U

RAS0 L

RAS1 L

R/W

UDSG

LDSG

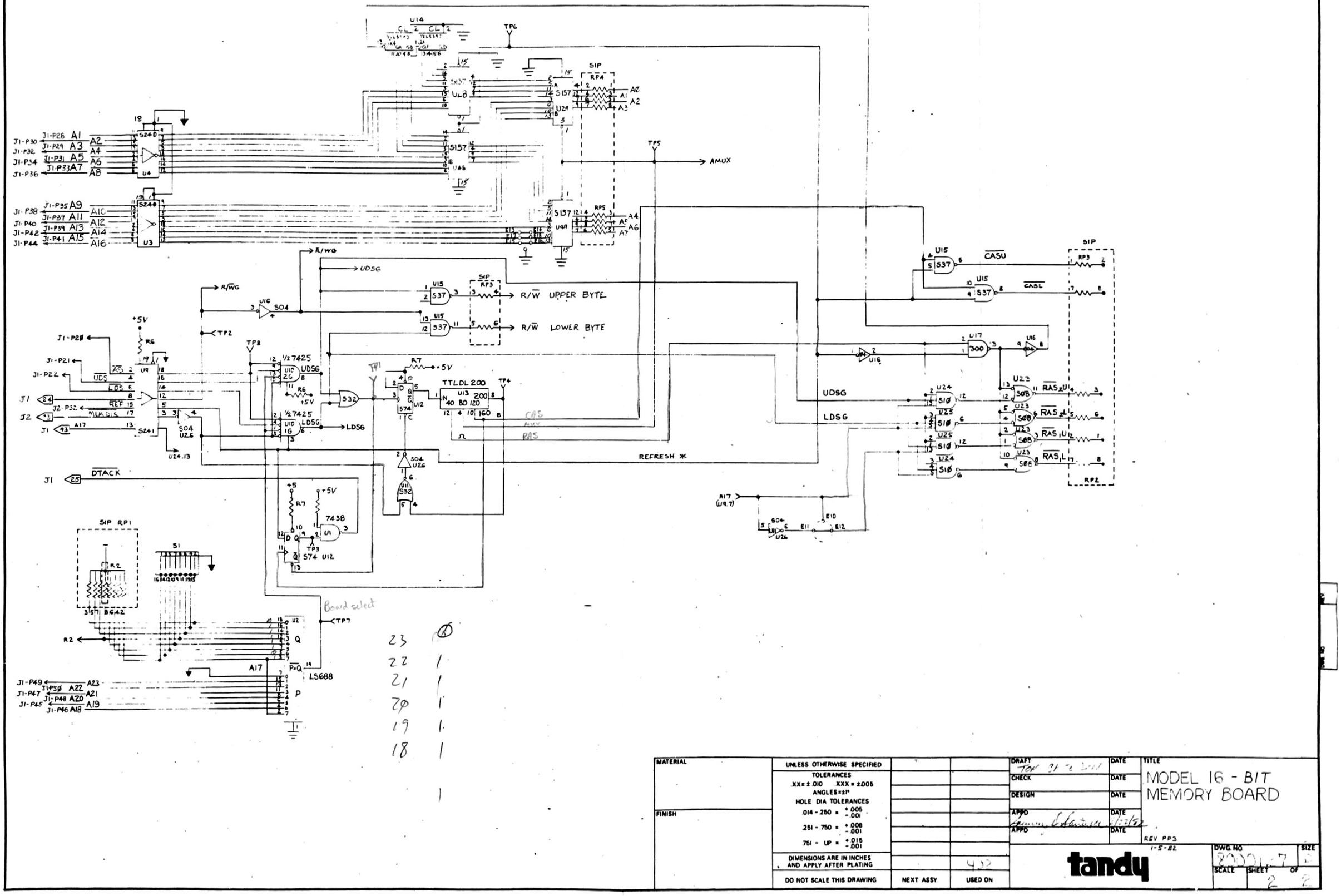
AMUX

AS

REFRESH

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT TOM CASTELLON	DATE 6-1-81	TITLE
	TOLERANCES .XX=±.010 .XXX=±.005 ANGLES=±1° HOLE DIA TOLERANCES .014-.250 = +.005 -.001; .251-.750 = +.008 -.001; .751-UP = +.015 -.001			CHECK	DATE	MODEL 16-BIT MEMORY BRD
FINISH				DESIGN	DATE	
				APPD	DATE	
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING			APPD	DATE	REV PP3
	DO NOT SCALE THIS DRAWING	NEXT ASSY.	USED ON 402	tandy	1-5-82	DWG. NO. 8300127 SIZE D
						SCALE SHEET 1 OF 2

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



23 0
22 1
21 1
20 1
19 1
18 1

1

MATERIAL	UNLESS OTHERWISE SPECIFIED			DRAFT	DATE	TITLE	
	TOLERANCES			CHECK	DATE	MODEL 16 - BIT MEMORY BOARD	
	XX = ± .010 XXX = ±.005			DESIGN	DATE		
	ANGLES = ±1°			APPD	DATE		
FINISH	HOLE DIA TOLERANCES			APPD	DATE		
	.014 - .250 = +.005 -.001					REV PP3 1-5-82	
	.251 - .750 = +.008 -.001						
	.751 - UP = +.015 -.001						
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING		422	tandy		DWG NO 8000-7	SIZE D
	DO NOT SCALE THIS DRAWING	NEXT ASSY	USED ON			SCALE	SHEET 2 OF 2