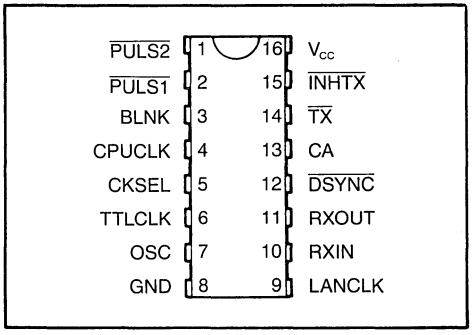
COM 9032
Local Area Network Transceiver
LANT

FEATURES

- ☐ Reduces chip count for COM 9026 ARCNET* implementations by 6-8 TTL chips
- ☐ Performs all clock generation functions for the COM 9026
- ☐ Compatible with the COM 9026
- ☐ Provides line drive signals for transmission
- ☐ Converts incoming serial receive data to NRZ data format
- ☐ Generates two 4 MHz general purpose clocks

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM 9032 local area network transceiver is a companion chip to the COM 9026 Local Area Network Controller (LANC) and will perform the additional functions necessary to allow simple interface to a transmission media for all ARCNET* (or equivalent) local area networks. Using a 20 MHz input clock, the COM 9032 will produce two, 5 MHz clocks for the COM 9026. The first 5 MHz clock is free running and will directly feed the CLK input of the COM 9026 (pin 19). The second 5 MHz clock has start/stop capability which is controlled by the $\overline{\text{DSYNC}}$ output of the COM 9026 (pin 36) and the received data input as required by the COM 9026 (pin 2). Two additional 4 MHz free running clocks are also generated on the COM 9032 to allow operation of other logic, a microprocessor, or an LSI controller.

During data reception, the COM 9032 will convert incoming serial receive data from the transmission media to NRZ form which will directly feed the RX input of the COM 9026 (pin 38). During transmission, the COM 9032 converts the transmit data from the COM 9026 ($\overline{\text{TX}}$, pin 37) into the waveforms necessary to drive opposite ends of the rf transformer used in the ARCNET* cable electronics shown in figure 2.

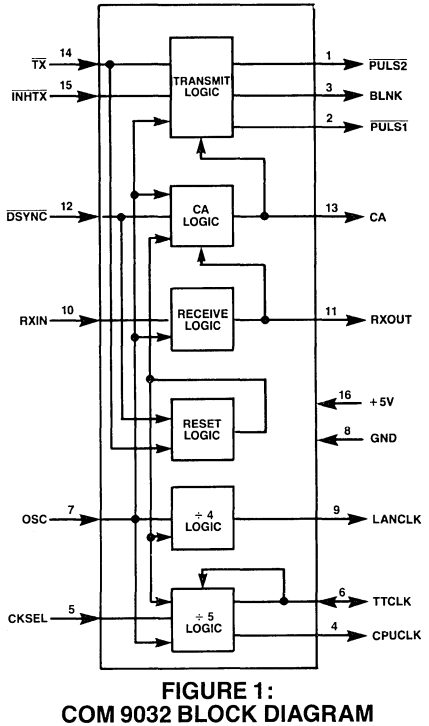
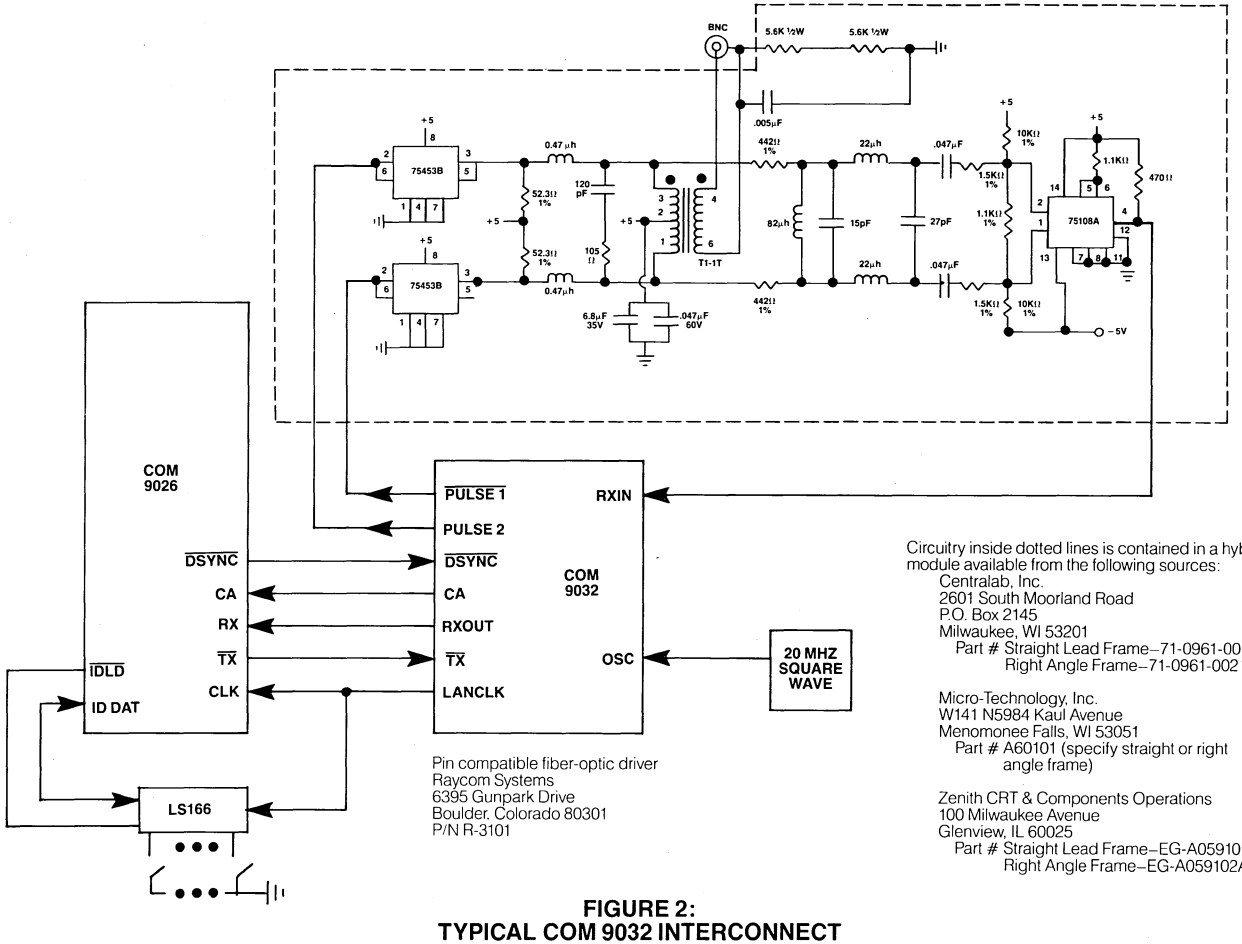


FIGURE 1:
COM 9032 BLOCK DIAGRAM

*ARCNET is a registered trademark of the Datapoint Corporation.



Pin compatible fiber-optic driver
Raycom Systems
6395 Gunpark Drive
Boulder. Colorado 80301
P/N R-3101

Circuitry inside dotted lines is contained in a hybrid module available from the following sources:

Centralab, Inc.
2601 South Moorland Road
P.O. Box 2145
Milwaukee, WI 53201
Part # Straight Lead Frame–71-0961-001
Right Angle Frame–71-0961-002

Micro-Technology, Inc.
W141 N5984 Kaul Avenue
Menomonee Falls, WI 53051
Part # A60101 (specify straight or right angle frame)

Zenith CRT & Components Operations
100 Milwaukee Avenue
Glenview, IL 60025
Part # Straight Lead Frame–EG-A059101A
Right Angle Frame–EG-A059102A

FIGURE 2:
TYPICAL COM 9032 INTERCONNECT

DESCRIPTION OF PIN FUNCTIONS

(Refer to figure 2)

COM 9026 INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
1, 2	PULSE 2 PULSE 1	$\overline{PULS2}$ $\overline{PULS1}$	$\overline{PULS2}$ and $\overline{PULS1}$ are two nonoverlapping negative pulses which occur every time the $\overline{TX}$ input is pulsed. $\overline{PULS2}$ and $\overline{PULS1}$ are used to feed an external driver as shown in figure 2.
3	BLANK	BLNK	When used with the circuitry shown in figure 2, this output should be left unconnected. The timing of this signal is shown in figure 4.
10	RECEIVE IN	RXIN	This input is the recovered receive data from the network. For each dipulse appearing on the network, the comparator shown in figure 2 will produce a positive pulse which directly feeds this input.
11	RECEIVE OUT	RXOUT	This output is the NRZ data generated as a function of the RXIN pulse waveform which directly feeds the RX input of the COM 9026 (pin 38).
12	DELAYED SYNC	$\overline{DSYNC}$	This active low input, which is asserted by the COM 9026, will halt the CA clock output.
13	CA	CA	This output is a 5 MHz start/stop clock that is halted when $\overline{DSYNC}$ goes active low and restarted by a low signal on the RXOUT output. This clock is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
14	TRANSMIT DATA	$\overline{TX}$	This input, which is asserted by the COM 9026, is the serial data transmitted by the node.
15	TRANSMIT INHIBIT	$\overline{INHTX}$	This active low input inhibits the $\overline{TX}$ signal from initiating transmit signals by forcing $\overline{PULS1}$ and $\overline{PULS2}$ to a high and BLNK to a low. This signal should be asserted during a power on reset condition.

SYSTEM CLOCK INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
4	CPU CLOCK	CPUCLK	This output is a 4 MHz free running clock capable of driving 130 pf with 30 nanosecond rise and fall times. It is identical to the TTLCLK input when CKSEL is high. When CKSEL is low, this output becomes the inversion of the signal that is fed into the TTLCLK input.
5	CLOCK SELECT	CKSEL	This input selects the clock interface option for the TTLCLK and CPUCLK. When this signal is high, both the TTLCLK and CPUCLK are identical 4 MHz free running clock outputs which are generated from the 20 MHz input clock (OSC) via a divide by 5 frequency divider. When this input is low, the TTLCLK pin becomes an input and the CPUCLK output will produce the inversion of the signal appearing on TTLCLK input.
6	TTL CLOCK	TTLCLK	This pin can be either an input or an output depending on the state of the CKSEL input. When CKSEL is high, a free running 4 MHz clock is ouput. When CKSEL is low, the pin becomes an input which drives an inverter that feeds the CPUCLK output.
7	OSCILLATOR	OSC	This input requires a 20 MHz clock.
9	LOCAL AREA NETWORK CLOCK	LANCLK	This output will supply the free running 5 MHz clock to the COM 9026, pin 19. It is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
8	GROUND	GND	Ground
16	+5 VOLT SUPPLY	V_{CC}	Power Supply

FUNCTIONAL DESCRIPTION

Transmit logic (refer to figures 2 and 4)

The COM 9026, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Refering to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to two, 100 nanosecond nonoverlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ are used to create a 200 nanosecond wide dipulse by driving opposite ends of the RF transformer shown in figure 2.

Receive logic (refer to figures 2 and 5)

As each dipulse appears on the cable, it is coupled through the RF transformer, passes through the matched filter, and feeds the 75108B comparator. The 75108B produces a positive pulse for each dipulse received from the cable. These pulses are captured by the COM 9032 and are converted to NRZ data with the NRZ data bit boundaries being delayed by 5 OSC clock periods as shown in figure 5. As each byte is received by the COM 9026, the CA clock is stopped by the COM 9026 (via $\overline{DSYNC}$) until the first bit of the next byte is received which will automatically restart the CA clock. The COM 9026 uses the CA clock to sample the NRZ data and these sample points are shown in figure 5.

Typically, RXIN pulses occur at multiples of the transmission rate of 2.5 MHz (400 nanoseconds). The COM 9032 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −55° to 150°C
Lead Temperature (soldering, 10 sec.) ..... 325°C
Positive Voltage on any Pin ..... +8V
Negative Voltage on any Pin ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGES					
V_{IH}	2.7			V	
V_{IL}			0.8	V	
OUTPUT VOLTAGES					
V_{OH1}	2.4			V	I_{OH} = −0.4 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs.
V_{OL1}			0.4	V	I_{OL} = 4.0 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs.
V_{OH2}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CPUCLK output.
V_{OL2}			0.4	V	I_{OL} = 0.1 mA, CPUCLK output.
V_{OH3}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CA and LANCLK outputs.
V_{OL3}			0.4	V	I_{OL} = 0.4 mA, CA and LANCLK outputs.
LEAKAGE CURRENT					
I_{11}			50	µA	TTLCLK input with CKSEL low.
I_{12}			10	µA	all other inputs.
INPUT CAPACITANCE					
C_{IN}			20	pf	
SUPPLY CURRENT					
I_{CC}			20	mA	at 20 MHz OSC frequency.

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
OSC Input					
t_{CY1}		50		ns	
t_{CH1}	20			ns	
t_{CL1}	20			ns	
CA, LANCLK					
t_{CY2}		200		ns	
t_{CH2}	75			ns	
t_{CL2}	75			ns	
t_{F2}			20	ns	
t_{R2}			20	ns	
TTLCLK					
t_{CY3}		250		ns	
t_{CH3}	110			ns	
t_{CL3}	110			ns	
CPUCLK (CKSEL is high)					
t_{CY4}		250		ns	
t_{CH4}	110			ns	
t_{CL4}	110			ns	
t_{F4}			30	ns	
t_{R4}			30	ns	
t_{DCK}			45	ns	for CKSEL low.
TRANSMIT TIMING					
t_{STC}	50	30		ns	
t_{HTC}	10			ns	
t_{DP}			60	ns	
t_{P1W}		$2t_{CY1}$		ns	
t_{WB}		t_{CY1}		ns	
t_{P2W}		$2t_{CY1}$		ns	
t_{RST}			40	ns	
RECEIVE TIMING					
t_{RS}	30			ns	
t_{RW}	10			ns	
t_{DO}			70	ns	
t_{RO}		$5t_{CY1} + t_{DO}$		ns	
t_{SSO}	10			ns	
t_{SSC}		20		ns	
t_{ROW}		400		ns	

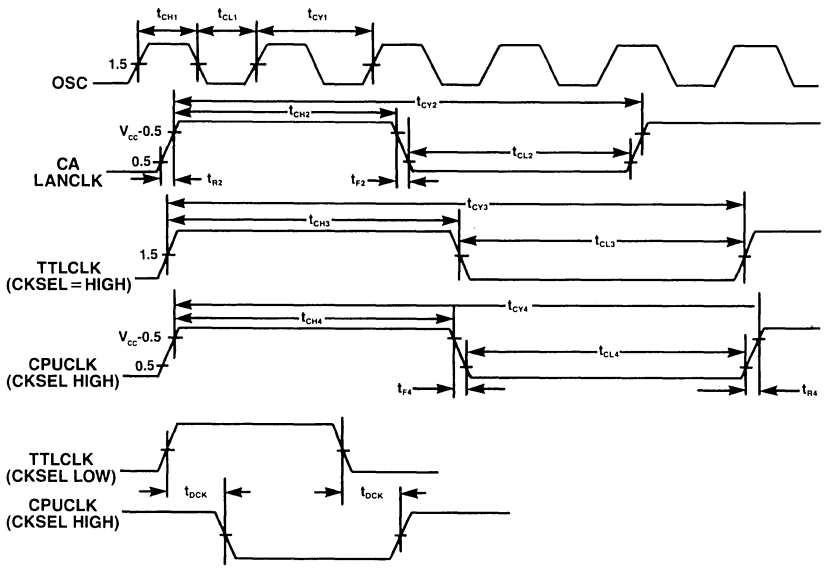


FIGURE 3: CLOCK TIMING

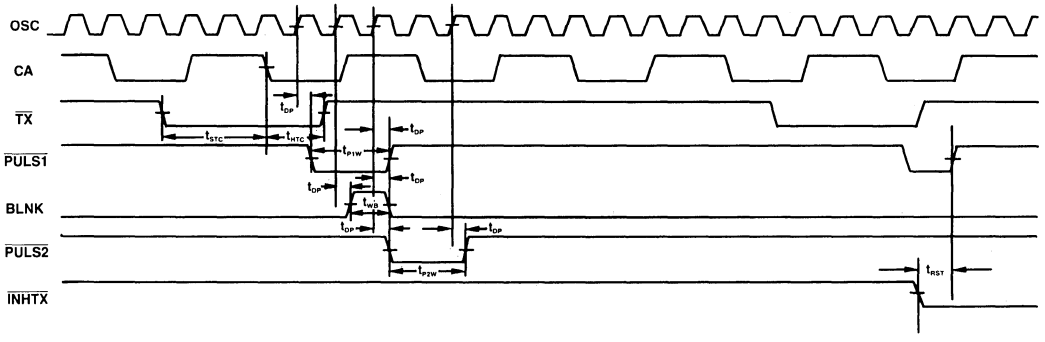


FIGURE 4: TRANSMIT TIMING PARAMETERS

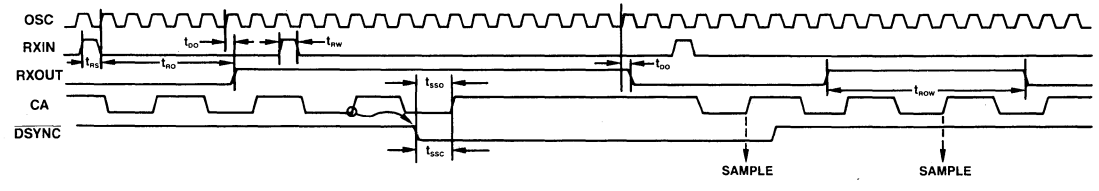


FIGURE 5: RECEIVE TIMING PARAMETERS

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 · TWX-510-227-8898