The magic of ARCNET is handled very simply, at least from a programmer's point of view. Since the Resources Interface Management (RIM) chip handles all of the ARCNET transmission and reception protocol, it is necessary for the host computer to interface to the RIM board in only four instances:

1) During RESET
2) To transfer data packets between the RIM buffer memory and the Z-8Ø memory
3) To read the status register or write to the interrupt mask register
4) To configure, enable, or disable the RIM functions

The RESET function does not require that the Z-8Ø access the RIM chip directly. Instead the MASTER RESET LINE from the computer is attached to the ARCNET PC board through the motherboard. This allows the ARCNET board and RIM chip to be reset at the same time that the rest of the computer system is being reset.

Data transfer between the Z-8Ø and the ARCNET buffer memory is handled directly by the Z-8Ø. Again, it is not necessary to access the RIM chip to allow data transfers. The Z-8Ø can read from or write to the ARCNET buffer memory without interference from the RIM chip.

Reading the RIM chip's status register enables the ARCNET control program to determine the present status of the RIM chip. Like most devices, we must not try to make the RIM chip do too many things at once. By checking the status register we can see if the RIM chip has received a data packet, or has finished transmitting the previous data packet.

The RIM CHIP STATUS REGISTER is interpreted as follows:

Bit Ø -- Transmitter Available -- If set (= "1") then the RIM chip is ready to accept a TRANSMIT command. If reset (= "Ø") then the RIM chip is presently in the process of transmitting a data packet.

Bit 1 -- Transmit Message Acknowledged (TMA) -- If set then the RIM chip has received a ACK signal to the previously transmitted packet.

Bit 2 -- Reconfiguration -- If this bit is set it indicates that the RIM chip has attempted a reconfiguration because the line receiver did not detect activity for more than 78 microseconds.

Bit 3 -- Test -- This bit is low for all normal operating conditions. If this bit is set this would indicate an unknown abnormal system operation.

Bit 4 -- Power On Reset (POR) -- If set this indicates that the RIM chip has received a Power On Reset from the computer.

Bit 5 -- ETS1 -- This bit reflects the current status of Pin 3.

Bit 6 -- ETS2 -- This bit reflects the current status of Pin 1.

Bit 7 -- Receiver Inhibited -- If this bit is set this indicates that a data packet has been received and deposited into the ARCNET RAM buffer

Writing to the Interrupt Mask Register allows the ARCNET control software to selectively program the RIM chip to generate interrupts under certain circumstances. Set the corresponding bit HIGH to enable the selected interrupts. The Interrupt Mask Register is programmed as follows:

Bit Ø -- Transmitter Available -- Generate an interrupt as soon as the transmit section is available, usually after completion of a data packet transmission.

Bit 1 -- unused

Bit 2 -- Reconfiguration -- Generate an interrupt if the reconfiguration timer exceeds 78 microseconds

Bit 3 -- unused

Bit 4 -- unused

Bit 5 -- unused

Bit 6 -- unused

Bit 7 -- Receiver Inhibit -- Generate an interrupt whenever a data packet reception is complete.

The RIM chip functions are programmed using one only six commands. Using these six commands allows the programmer to write software that completely controls the ARCNET system. The commands are:

1) Disable the transmitter. Any PENDING data transmissions are disabled. If a data transmission is in progress it will be completed. Only data packet transmission are disabled. Token passing and acknowledgement are not effected.

2) Disable the receiver. Any further attempts to receive data packets will be answered with a NACK packet. If a packet reception is in progress it will be completed. Token passing and acknowledgement are not effected.

3) Enable data packet from buffer page. This command points the RIM chip to any one of the available RAM buffer pages, and enables the transmit section if the RIM chip. The actual data packet transmission will not take place until the RIM chip next receives the "token".

4) Enable Data Packet to buffer page. This command points the RIM chip to any one of the available RAM buffer pages, and enables the receive section of the RIM chip. The RIM chip will not receive data EXCEPT that data which is specifically addressed to it.

5) Define memory configuration. This defines the ARCNET RAM buffer as being either 1K or 2K in size. If the RAM buffer is only 1k the RIM chip is capable of receiving only 256-byte or shorter packets. If the RAM buffer is 2K the RIM chip may receive up to 512-byte packets.

6) Clear flags. This command is used to clear the Power On Reset flag, the Recon Timer flag, or both.

ARCNET PACKETS

ARCNET works in a manner similar to, but not identical to, standard RS232 asynchronous data communications. There are four major differences:

1) ARCNET operates at a 2.5 Megabaud (2.5 million bits per second) data transfer rate.

2) ARCNET signals are not RS232 standard compatible; instead, they require a special RG62 coaxial cable.

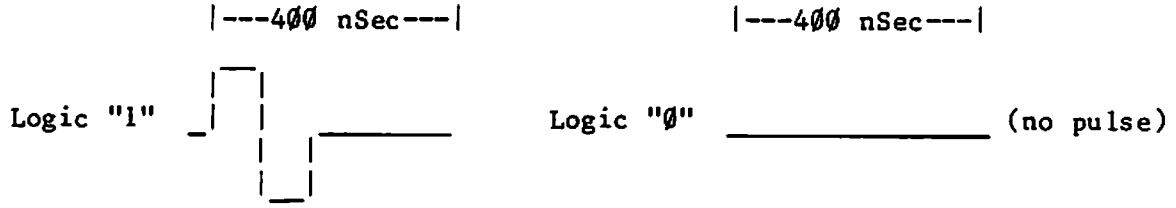
3) ARCNET signals use a Return to Zero (RZ) pulse to transmit a "1" bit while RS232 uses Non Return to Zero (NRZ) DC levels to indicate "1s" or "Øs".

4) True asynchronous communications may have a variable time between transmitted characters. ARCNET uses a well-defined time between transmitted characters.

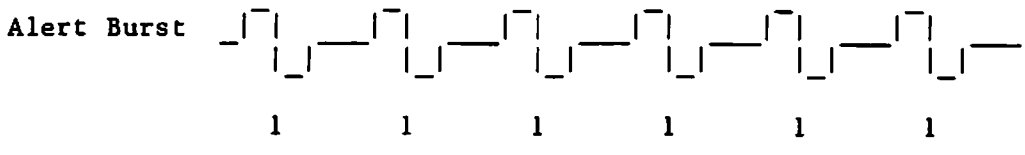
Otherwise, ARCNET and RS232 both use binary coded transmissions and each byte transmitted is framed by a set number of START and STOP bits.

The ARCNET transmission is defined to idle in the Logic "Ø" condition, therefore, any change in level from a "Ø" to a "1" will indicate activity on the line. In fact, this very idea is used by the ARCNET Active Hub to switch the nodes between receive and transmit.

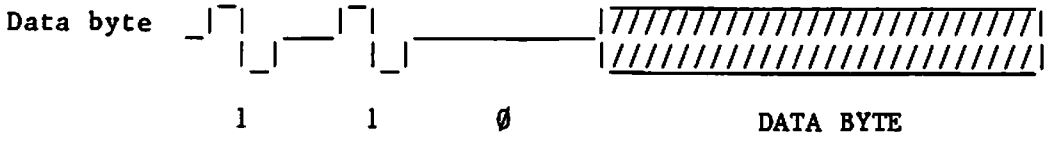
The ARCNET RIM chip encodes data using a bipolar pulse scheme -- a "1" bit is defined as 1ØØ nanoseconds of a positive pulse followed by 1ØØ nanoseconds of a negative pulse. This provides a total pulse time of 2ØØ nanoseconds. By using identically timed but opposite polarity pulses (RZ format) any residual DC charge in the cable is eliminated. The bit cell time is twice as long - 4ØØ nanoseconds - resulting in the 2.5 MBaud transmission rate.



To synchronize all units involved in a transmission, and to assure that no characters are missed, the RIM chip supplies an ALERT BURST as part of every packet, regardless of the type or purpose of the packet. The Alert Burst consists of six successive "1s".



The ARCNET RIM chip also supplies framing bits for each eight-bit character sent. These bits are similar to the start and stop bits used by RS232 communications, but the ARCNET uses no stop bit. Each character sent is preceded by two "1s" and one "Ø". This results in a an eleven-bit transmission "byte".



We now know that it takes 4ØØ nanoseconds to transmit one bit, and each byte transmitted consist of eleven bits. It therefore takes 11 x 4ØØ nanoseconds, or 4.4 microseconds, to transmit one byte. It takes 6 x 4ØØ nanoseconds, or 2.4 microseconds, to transmit the Alert Burst. This is all very defined and fixed. Unlike other asynchronous transmissions, the time between data bytes is fixed. Therefore, if we know exactly how many bytes are in a data packet we can predict exactly how long it will take to transmit that packet.

There are only five different packets handled by the ARCNET system. There are four CONTROL packets including the TOKEN which is passed around the system, and one DATA packet which may be of any length up to 512 bytes.

INVITATION TO TRANSMIT (the TOKEN)

Alert Burst	EOT Ø4 hex	DID	DID

This is the TOKEN which is "passed" around the system. If an ARCNET unit does not control the token it can not transmit a data packet. A unit that does not control the token will still transmit acknowledgement of reception of packets addressed to it. Note that the Destination Identification (DID) number is repeated.

It takes 2.4 microseconds for the Alert Burst and 4.4 microseconds for each of the three data bytes, or a total of 15.6 microseconds to transmit this token.

FREE BUFFER ENQUIRY (FBE)

Alert Burst	ENQ Ø5 hex	DID	DID

This packet asks the Destination unit (#DID) if it has a free RAM buffer available on the ARCNET PC board. If the DID unit has a free memory buffer it will transmit an ACK packet in return. If there is no buffer available the DID will transmit a NACK packet.

This packet takes 15.6 microseconds to transmit.

ACKNOWLEDGE (ACK)

Alert Burst	ACK Ø6 hex

This packet is sent to acknowledge the receipt of a transmitted packet from another unit. It is used to acknowledge that there is a free buffer available. It is also sent after a data packet has been received and the cyclic redundancy check (CRC) verified.

It takes 2.6 microseconds to transmit the Alert Burst and 4.4 microseconds for the ACK signal, for a total of 7 microseconds necessary to transmit this packet.

NEGATIVE ACKNOWLEDGE (NACK)

Alert Burst	NACK 15 hex

This packet is sent if there is not a free RAM buffer available, or if a data packet is received with an incorrect CRC value. The operating software will determine how to handle these situations.

This packet takes 7 microseconds to transmit.

DATA PACKET

Alert Burst	SOH Ø1 hex	SID	DID	DID	BYTE COUNT A	BYTE COUNT B	n BYTES of DATA	CRC1	CRC2

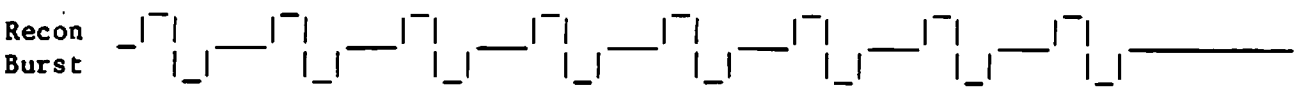
This packet contains the actual data to be sent. The Alert Burst is followed by the ASCII code for Start Of Header to indicate the following information is a Data Packet. The Source Identification number (SID) of the transmitting unit follows, and then the Destination ID (DID) is transmitted twice.

The number of bytes in the actual data packet is sent in the next two bytes. If the data packet is 256 bytes or less then BYTE COUNT A contains the 2's complement of the actual byte count, and DATA COUNT B is missing. If the data packet is greater than 256 bytes but less than 513 bytes then BYTE COUNT A contains ØØ and BYTE COUNT B contains the 2's complement of the number of bytes to be sent.

Following the Byte Count bytes is the actual data to be sent. This consists of up to 512 bytes, as indicated by the Byte Count bytes. Once the correct number of bytes are transmitted a two byte (16 bit) Cyclic Redundancy Check (CRC) is transmitted.

The time necessary to transmit a data packet depends on the size of the packet. The Alert Burst requires 2.6 microseconds, and the SOH, SID, DID bytes, Byte Count bytes, and CRC bytes require 4.4 microseconds each, for a total of 37.8 microseconds maximum in "overhead". Each byte in the packet requires 4.4 microseconds, or a maximum of 2252.8 microseconds for a 512-byte packet. Adding this to the overhead figure provides a maximum data packet time of 229Ø.6 microseconds, or approximately 2.3 milliseconds to transmit a 512-byte data packet. A 256-byte packet would take approximately half as long, or almost 1.2 milliseconds.

RECONFIGURATION BURST



1 1 1 1 1 1 1 1 Ø

(repeated 765 times)

The RECONFIGURATION BURST is transmitted under two conditions:

1) Immediately after Power On or Reset
2) If a RIM chip has not received the TOKEN for 84Ø milliseconds

The nine bits of the recon burst are repeated 765 times for a total burst transmission time of 3Ø294 microseconds, or approximately 3Ø milliseconds. This time is guaranteed to be longer than any possible packet (by at least a factor of 1Ø). Since this burst is so very long it will destroy any attempts to pass the token, causing the transmission line to appear momentarily dead. When this happens each RIM chip goes into its RECONFIGURATION MODE, and in the process of reconfiguring the new (or lost) unit will insert itself into the token passing chain.

It appears that system reconfiguration would take a long period of time, at least more than 84Ø milliseconds. However, while one unit is waiting for the 84Ø milliseconds the remaining units are still active. The ARCNET system is disrupted only for the 3Ø milliseconds of the Recon Burst, and for less than 6Ø milliseconds during the system reconfiguration period. The ARCNET system is actually disrupted for less than 1ØØ milliseconds total during a system reconfiguration.

MANDATORY TECH TIPS TO CHECK BEFORE INSTALLING ARCNET

Model II:

II:2 Memory Board Jumpers
II:5 Video modifications
II:25 POR resistor modification
II:26 DMA mod to Rev C or lower CPU
II:29 6ØØ8 power supply adj.
II:31 Memory jumpers
II:32 CPU jumpers
II:37 Video modifications

Model 16:

16:3 Clock Modifications
16:5 Reversed C41
16:15 6ØØ9 power supply modifications

Model 12/16B:

12/16B:2 Reset failures
12/16B:5 Motherboard modification
12/16B:6 DMA modifications
12/16B:9 Jumper settings
12/16B:1Ø Cooling modification
12/16B:14 Printer not ready

Hard Drives:

HD:1 Switch settings
HD:2 Wrong potentiometer
HD:4 Clock modification
HD:6 Stepper gets lost
HD:9 Tie Connectors
HD:1Ø Resistor pack modifications
HD:11 Board differences
HD:12 Modified boards

ARCNET:

ARCNET:2 Transistor and jumper modification
ARCNET:3 COM9Ø26 chip replacement
ARCNET:4 Jumper settings
ARCNET:6 Faulty DIP switches

Beware of Zilog CTC chips