Radio Shack®

Technician Series

TRS-80®

ARCNET TECHNICAL INFORMATION

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ARCNET™ INFORMATION

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FOR INTERNAL USE ONLY

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This ARCNET™ installation manual has been prepared based on actual installations in the field as well as the Tandy Center. It is very important that this manual be read completely and understood before attempting an ARCNET™ installation. This document is intended to assist service personnel in the planning of ARCNET™ installations. It is for internal use only and is not to be given to customers.

Table of Contents

WHAT IS ARCNET™ ?

ARCNET™ is one answer to the problems of Local Area Network (LAN) systems which are rising in popularity as computerized systems become more readily available. Local Area Networks allow a reasonable alternative to mainframe time sharing systems by using distributed processing.

Distributed processing, on an elementary level, allows high work throughput with a minimal system. In the LAN system, each unit can be no more than a single microcomputer with one disk drive. Printers, multiple disks, or hard disks are unnecessary at each individual work station. By distributing processing power and equipment around the LAN, each unit in the LAN can effectively have access to printers or mass storage (hard disks, etc.) without actually having to purchase the extra equipment for each unit. On a more advanced level, distributed processing allows each unit in the LAN to access files and data bases created by another unit, and in some cases simultaneously with another unit.

Even more importantly, the LAN supplies each unit with actual processing power. Access to any file or data base is very quick, usually appearing as though the unit actually had the desired file at its location. Once the file is obtained, the individual unit has the power to process the information as necessary. Waiting for the mainframe to process data is eliminated, thus eliminating the main cause of long lag times often associated with true time sharing systems. The other cause of long lag times, waiting for the main frame to become "free" for a transmission, is also greatly reduced as we shall see.

LAN PROTOCOL

ARCNET™, as was said, is one method of achieving a Local Area Network. Another is CSMA-CD, Carrier-Sense Multiple-Access with Collision Detect. Regardless of the system, the basic idea is the same. Each unit sends bursts of information, called PACKETS, into the line (cables). This packet has attached to it an address of a particular unit. The receiving unit, upon detecting a packet addressed to it, receives the packet and acts on it accordingly.

Some problems surface with the CSMA-CD system. First, each unit must "listen" to the line to detect a break in other transmissions before it can send its packet. If two units are waiting to send, and both detect the same break, they will most likely send their packets simultaneously. This results in a packet collision, hence the Collision Detect provision. Although quite sophisticated, CSMA-CD still results in many retries. If there are many active users on a LAN, CSMA-CD may actually show a slowdown in systems throughput.

ARCNET™ involves a different method of determining who will use the line at any given moment. This system, called TOKEN PASSING, totally eliminates any packet collisions and therefore transmission retries, by guaranteeing each active unit a turn to use the line. This assures that system throughput always remains high, even with a large number of active users.

Token passing is the very heart and soul of the ARCNET™ system. The TOKEN is actually a specialized data packet known as an INVITATION TO TRANSMIT. One unit receives a token from another unit that has just finished transmitting its packet. The unit receiving the token may now transmit its packet and then pass the token to the next unit, or it may simply pass the token without transmitting if it has nothing to transmit. In this matter each unit is guaranteed a turn to transmit a data packet on a regular basis.

A TOKEN PASSING SYSTEM

Let's see how the token passing works in a small ARCNET™ system. Figure 1 shows an ARCNET™ Active Hub with five Application Processors (AP) accessing one File Processor (FP). Each unit in the ARCNET™ system is given a unique Indentification Number (ID) when the unit is installed. Any one ARCNET™ system may have up to 255 units attached, each having a unique ID from 1 to 255 (unit number Ø is not allowed).

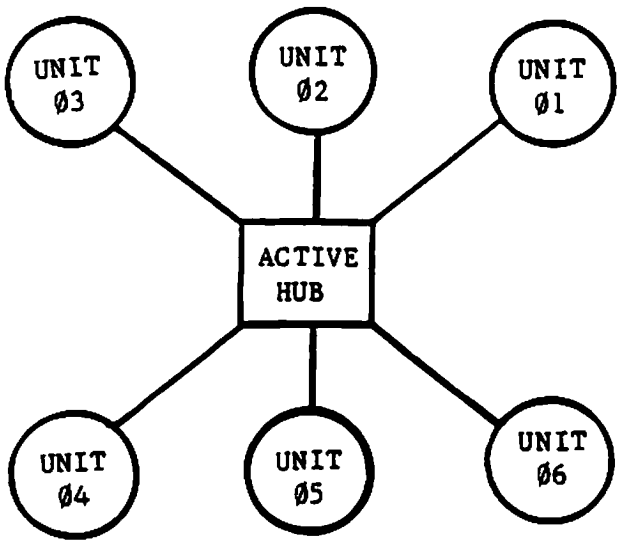


FIGURE 1

Note that our system example has only one FP. In larger systems it is quite common, in fact recommended, that there be more than one FP per network. This further distributes the processing load, allowing faster access to any given file since it is unlikely that all users would want to access the same file at the same time. However, the function of the **ARCNET™** boards is identical in all units. The FP or AP functions of any one unit is totally dependent on the system software loaded.

Normally, the FP would be the first unit turned on, although the exact order of the system is not ultimately important. With the exception of the FP, any unit may be in or out of the system as needs require. The FP is dedicated to the task of handling mass storage (hard disk) can cannot be used for any other purpose.

When any **ARCNET™** board is first activated, it must make itself known on the system. This is known as **RECONFIGURATION (RECON)**. The first unit powered up will not find any tokens to be passed. It then checks its own ID, increments this number by one, and then sends a token to this **Next ID (NID)**.

This unit now waits for the unit at NID to acknowledge that it has received the token. If there is no unit at NID, the active unit will again increment NID and try again. This process continues until the active unit receives an **ACKNOWLEDGE (ACK)**. Note that if there are NO other units on the system, the active unit will continually try to reconfigure the system and contact the remaining 254 units until it is turned off or another unit comes on line.

SYSTEM RECONFIGURATION

Let's now assume that unit Ø2 has been activated and established communications with unit Ø1. We now have a complete system consisting of two units. Now, unit Ø5 wishes to come on line. Since a complete system is now operational (units Ø1 and Ø2), unit Ø5 must reconfigure the system. It does this by "destroying" the token.

To destroy the token, unit Ø5 transmits a packet that is guaranteed to be longer than any other packet. This will interfere with any packets being transmitted. Note that only the packet is destroyed. Information at every unit is kept intact until the transmitting unit receives the ACK signal from the unit being transmitted to, or **Destination IDentification (DID)**.

Since all packets have been destroyed, units Ø1 and Ø2 have broken communication. The transmitting unit has not received an ACK signal, and the DID unit has not received a packet. The line goes dead. Units Ø1, Ø2, and Ø5 now wait for 78us, and each unit then proceeds to go into the **RECONFIGURATION** mode.

Each unit continues to wait for a time that is determined by its ID number. The unit with the highest ID will time out first. Unit Ø1, the lowest possible ID, would time out last after approximately 38ms.

The first unit to time out begins to pass the token, starting with an NID of its own ID plus one. In our small system, unit Ø5 will time out first and begin to pass the token. Units Ø1 and Ø2, sensing coherent activity on the line, will begin to wait their turn. Unit Ø5 first passes the token to unit Ø6, which doesn't exist. After waiting a suitable length of time for the ACK from unit Ø6 (which never comes), Ø5 then increments its NID, and tries unit Ø7. This process continues until unit Ø5's NID is Ø1, at which time unit Ø1 sends an ACK signal that it has received the token. Unit Ø5 now stores Ø1 as its NID and relinquishes the token to unit Ø1.

Unit Ø1 begins to pass the token, quickly finds unit Ø2, and successfully passes the token to Ø2. Unit Ø2 tries to pass a token to unit Ø3, and then Ø4, finally locating unit Ø5. The network is now again complete with three units functional.

The reconfiguration process takes MUCH longer to read than it does to happen. While any new unit requesting to come on line (like unit Ø5 above) must wait approximately 85Ø ms before destroying the token, other units on line can continue processing during this time. Once the token is destroyed, the reconfiguration process is completed in typically less than 6Øms! Any one unit coming on line is therefore reconfigured into the system in less than one second, and without noticeable interference to any other unit presently one line!

Let us now suppose that we have all six units on line and functioning. Let us also suppose that unit Ø6 wishes to leave the system. For unit Ø6, it simply removes itself from the line. However, unit Ø5 still contains Ø6 as its NID. When unit Ø5 is ready to pass the token, it does not receive an acknowledge. After a suitable wait for an acknowledgement, it increments its NID (now to Ø7) and tries again. This process is repeated until Ø5 receives an acknowledgement from unit Ø1. Unit Ø5 now has an NID of Ø1, and the system is again complete -- but without need for a reconfiguration.

A RUNNING SYSTEM

During normal system operation things run much smoother and faster (as if the above wasn't fast enough!). During reconfiguration, each unit establishes contact with the next ID on line. This is stored as the NID. Since each unit has stored its NID, the token is passed directly to this unit as long as this unit remains on line.

When any unit receives the token, it checks to see if it has a packet to send. If so, it first transmits a **FREE BUFFER ENQUIRY (FBE)** to the unit to which it wishes to send the packet. Note that any unit can transmit to any other unit if it has the token. The unit to which the FBE is addressed (DID) then checks to see if it has a free memory buffer available. If it has a free buffer then it sends the ACK to the unit requesting to send. If there is no free buffer then it sends a **Negative Acknowledge (NAK)** to the unit requesting to send.

If the unit with the token receives the ACK signal, it transmits its packet and waits for another acknowledge that the unit has received the packet. If it receives the NAK (no free buffer), it simply passes the token to the next unit. As well, if the unit with the token has no packet to send, it passes the token to the NID.

As you can see, the working **ARCNET™** system is smart. Each unit knows the NID of its neighbor, so time is not wasted waiting for units which are not on line. As well, each unit is guaranteed a time to transmit any information. Each individual unit determines whether or not it wishes to send, and passes the token when it is done. Also, no information is lost since each packet sent requires an acknowledge from the unit to which the packet is addressed both before the packet is sent and after.

SYSTEM TIMING

In the above discussion, we've mentioned things like "after a suitable wait". What is a "suitable wait", or put another way, "How fast is ACRNET™?"

One determining factor is the data transmission rate of the system, or baud rate. The **ARCNET™** board sends tokens or data packets at approximately 2.5 Megabaud -- 2.5 million bits per second!

Since **ARCNET™** is such a high speed system, essentially working in the RF region, things such as propagation delay and unterminated lines must be considered. One of the more important timings of an **ARCNET™** system is propagation delay. Considering the propagation delay of a system using RG62 type coaxial cable, no two units can be more than 31us apart, or approximately four miles.

Since any two units may be up to 31us apart, and any unit sending a packet must wait for an acknowledgement to come back, a unit must wait approximately 62us to be sure that it will not receive any signal from the unit to which it sent a packet. Also allowing for line reflections to cease (almost 5us each way) and a small allowance for error, the total time comes to approximately 74us.

This is the timing a unit used when waiting for acknowledgements from another unit. If a token is to be passed the unit will wait 74us for the ACK signal. If no signal is received this time a unit will assume that its NID is invalid, and will increment the NID and try again. This is the sequence of events used when an active unit leaves the network. If a data packet is to be sent the unit will wait 74us for the ACK signal and then retry the transmission, repeating the process up to 16 times before finally passing the token without transmitting. Note that this situation is an error, and will be handled appropriately by the system software.

Since token passing is the key to **ARCNET's™** efficiency, how long does it take to pass a token? Answer: Almost 28us. At this speed, a full system of 255 units could pass a token completely through the system in only 7 milliseconds. Of course, this figure does not include any propagation delay times. Even if all units on the system are separated by the maximum 31us the token can be passed completely through the system in only 26 milliseconds!

The token is actually the shortest communication to be sent. Data packets take somewhat longer. In fact, a 256-byte data packet takes approximately 1.2 milliseconds to transmit. At this rate, an **ARCNET™** system could handle 833 data packets per second. However, tokens must still be passed after each transmission, so system activity is actually around 400 to 500 packets per second, or two transmissions per user per second.

Still, this figure assumes 256-byte packets coming from 255 units which wish to transmit every time they receive the token. In actual practice many data packets are shorter than 256 bytes, most systems will consist of significantly less than 255 units, and not all units will wish to transmit all the time. This significantly increases the throughput to or from any individual unit, making the **ARCNET™** system appear to operate almost instantaneously to any individual user.

ARCNET™ HARDWARE

Obviously, the **ARCNET™** protocol does not just "happen". What makes it go? To handle all of the packets and timing and information is the job of the **Resource Interface Module (RIM)**. The RIM device is a special Large Scale Integration (LSI) chip designed especially for this purpose. The RIM is a dedicated processor in its own right. It only requires a small amount of external memory of its own for data buffers (typically 2K bytes), and necessary interfacing circuitry to the host computer.

Since the RIM is a dedicated processor, the host computer has to concern itself only with making sure that the buffers are loaded with any messages to be sent, and making sure any messages received are recovered and acted upon. The RIM handles all signal processing, waiting for tokens or packets, and handling all transmit and receive functions. Since the host processor is not tied up with these functions, more time is left for actual information processing.

Another important piece of the **ARCNET™** system is the **Active Hub.** Although the Hub is not "smart" (it has no processor of its own) it does perform some rather interesting functions.

The Active Hub is basically a repeater for the system. Each Active Hub contains a separate receiver and transmitter for each of the eight connections to the Hub. The Hub enables all receivers until one unit starts to transmit, at which time all other receivers are disabled, and the output of the active receiver is channeled to all other remaining transmitters.

In any cable transmission system there is a certain amount of line "reflections", not unlike standing waves found in radio transmission systems, and sharing common causes as well. In a properly designed transmission system, no "loose ends" may be left. All cables or taps (connections for future use with no unit attached) must be properly terminated at all times. Any cable or tap not terminated can "reflect" signals sent out over the system. A sufficient number of reflections from several different unterminated sources could possibly overpower the actual data transmission causing lost or erroneous data.

The **ARCNET™** Active Hub serves its second duty by making each tap the Hub supplies look like an ideal tap --ie. properly terminated at all times. The receivers and transmitters inside the Hub are all electrically identical to those found on the **ARCNET™** board. Therefore, any unit connected to the Hub is connected through an ideally terminated cable.

However, the unused taps in an **ARCNET™** Hub may be connected to a length of cable, or nothing at all, supplying an improperly terminated line. Therefore, the Active Hub waits for a period of approximately 5us after a transmission finishes before it enables all receivers to pick up the next transmission. Since line reflections will depend on the length of the unterminated line, this 5us time allows a maximum cable length between two Active Hubs or an Active Hub and an **ARCNET™** board of 2,ØØØ feet.

Passive Hubs may also be found in an **ARCNET™** system. Unlike the Active Hub, the Passive Hub has no "smarts" of its own. This means that each tap MUST be terminated for proper operation of the system. The Passive Hub is supplied with proper terminators to be attached to the unused taps.

ARCNET™ SOFTWARE

Each **ARCNET™** board is identical to all others in the system, with the exception of its ID number. The ID number is set with a set of small DIP switches. An **ARCNET™** board does not care if it is used as File Processor (FP) or Applications Processor (AP). Whether a unit is an AP or FP is totally a function of the system software loaded when the unit is first turned on, or after a RESET.

The **APPLICATIONS PROCESSOR (AP)** is a unit at which an operator actually runs a program. Some users may prefer to call these units TERMINALS, but each AP is actually a stand alone processor, capable of actually running a program and processing data.

The ARC8ØFP program is the heart of the AP software, It provides the necessary interfacing to the RIM to allow the unit to work within the **ARCNET™** network. However, the presence of the ARC8ØAP software does not guarantee that any given program will run with **ARCNET™**. Some programs may have to be significantly patched, or rewritten, to work in the **ARCNET™**system.

The **FILE PROCESSOR (FP)** is responsible for handling the information stored on the mass storage, usually 1 or more hard disks. Due to this extremely important function, the FP can not be used for any other function. Its sole use is to receive, transmit, and manipulate the data for the AP units.

The FP makes use of the ARC8ØFP software. In many ways ARC8ØFP is similar to ARC8ØAP. Interfacing to the RIM is virtually identical in either case. However, ARC8ØFP must interface to the Hard Disk Operating System, and help keep track of which unit is using what sector of what file on what hard disk. No simple task, even in a small system!

For this reason, it is recommended that large systems use more than one FP. It is also recommended that like files to kept at the same FP. In a large **ARCNET™** system, one FP may be dedicated to units running SCRIPSIT, one FP to units running PROFILE, and one FP to units running general bookkeeping programs. The reasoning for this is that no one FP is trying to manage the files for all APs. This is the whole purpose of distributed processing, and will generally allow higher information throughput.

ARCNET™ System Overview

The **ARCNET™** communication system is a system by which 255 Model II's, Model 12's, Model 16's, Model 16B's, or Model 16B+'s can share floppy disk drives, hard disk drives, and printers. As you can imagine, installation of this system can become a very complicated process. **The installation can only be a success if there is cooperation between the customer, the selling store, and the shop responsible for the installation.** This entire document has been written for the shop which must install the system and is intended to be used as a checklist only. The steps for successful system installation are as follows:

I) **Define the System.** Get together with the customer and determine the number of computers he intends to install. Determine which model will be used as the File Processor and the type of peripherals to be attached. Make sure the customer understands the following facts:

   A) The File Processor computer is a dedicated unit. While in the file processing mode it can not be used for anything else; i.e. Scripsit, Profile.

   B) When using the Model II in the **ARCNET™** system a 16K RAM expansion board (26-65Ø3) must be used if there is no hard disk drive interface board (26-415Ø/52) or Model 16 Enhancement Kit (26-6Ø1Ø) installed, because the TRSDOS 4.X uses this memory to load. The Model II will require modifications before it can be used in the **ARCNET™** system (see the **ARCNET™** Board Installation Instructions).

II) **Define the floor plan.** If possible, acquire a copy of the blue print which shows the floor layout. At the very least make a sketch of the floor plan. Make sure the floor plan contains the size of each room and don't leave out closets.

III) **Redefine the system.** Have the customer draw in his computer locations on the floor plans. Make the customer aware that a dedicated, isolated ground, AC outlet should be provided for each computer and Active Hub. A grounded three outlet plug is minimum requirement and must be provided. Now the distance between computers can be determined. Draw in the cable layout as efficiently as possible. The addition of hubs must now be made keeping in mind the following facts:

NOTE:

Cable path is defined as the total cable length, including any Passive Hubs, between two units.

Unit, as used in this text, is defined as anything connected to a Passive or Active Hub's ports.

A) A Passive Hub is a device used to match impedance for four cable connections. It can be used to link up to four units together provided the total cable length for any cable path does not exceed 2ØØ feet.

B) An Active Hub is a device which receives, amplifies and transmits the signal for eight cable connections. It may be used to link up to eight units together. Maximum cable length for an Active Hub is 2ØØØ feet unless there is a Passive Hub in the cable path.

C) A 93ohm Terminator must be placed on any unused connectors on the Passive Hub (supplied with the Passive Hub).

IV) **Make a list of materials.** Now that the system has been accurately defined it is possible to make a list of materials needed for the installation. The list should include the following:

A) Amount of RG62 cable needed (Number of feet) including ten feet of slack for each station. Note cable can be purchased in ready to use lengths of 2Ø feet (26-651Ø), 5Ø feet (26-6511), 1ØØ feet (26-6512), and in bulk of 5ØØ feet (26-6513).
B) Number of BNC connectors needed (278-1Ø4).
C) Number of Passive Hubs needed (26-65Ø4).
D) Number of Active Hubs needed (26-65Ø8).
E) Number of ARCNET™ Boards needed (26-65Ø1).
F) Number of 16K expansion boards needed (26-65Ø3).
G) Number of ARCNET™ File Processor software packages needed.

V) **Install the system.** Installing the system is done in seven steps:

A) Have an Electrician pull the cable. **NOTE: Radio Shack personnel will not pull the cable. This must be provided by the customer.** The cable should be pulled from one location to the next in grounded conduit (this will vary because of individual city building codes). This should be a dedicated conduit with nothing but **ARCNET™** cables running through it. AC lines should be avoided if at all possible. Keep in mind that enough slack must be left at each computer location to add a little flexibility to the positioning of the computer (ten feet). Each cable end should be marked with a durable tag showing where the other end of the cable is located. This will make future troubleshooting easier. Cooperation between the electrician and the installing technician is strongly advised.

B) Install the BNC connectors. The BNC connectors are to be installed by Radio Shack personnel only (except where local building codes forbid it). See Technical Bulletin **ARCNET™:Ø1**.

C) Check reliability of cables. Each cable should be checked for opens. This is done by shorting the center conductor to the shield using a jumper clip and going to the other end of the cable and measure the continuity between the two. There should be a short or, in the case of very long cables, a small resistance measured. Then remove the jumper clips. Each cable should then be checked for shorts. This is done by measuring the continuity between the center conductor and the shield. There should be a reading of infinity between the two. This check is extremely important.

D) Install the **ARCNET™** boards. See the **ARCNET™** Board Installation Instructions on page 18.

E) Install all the computers and the hubs. When installing a large system it is best to have two technicians to do the job. A dedicated Model II with an **ARCNET™** board installed makes system testing much easier. If there are no phones at each unit location "Walkie Talkies" may be needed because system testing requires communication between two technicians. The system should be tested using ARCTST each time a new unit is added to the system. If testing is post-poned until the entire system is installed it would be very difficult to locate 1 bad unit of 255.

F) Install File Processor software. First format the hard disk using the TRSDOS version that comes with the FP software package (4.3.11 or higher). When the format is complete hit reset and boot off the hard disk. After entering the date and time and with "TRSDOS II Ready" displayed type in **DO MOVEFP** and hit ENTER. When this process is complete the File Processor software is installed on the hard disk. At "TRSDOS II Ready" type in **ARC8ØFP** and hit ENTER. This will enter the computer into the ARCDOS operating system. When the prompt of **CI>** is displayed type **START FP** and hit ENTER. The File Processor is now ready to communicate with any Application Processor.

G) Install Applications Processor Software.

All that is involved in starting up the Application Processor is booting the floppy disk supplied with the **ARCNET™** board. After entering the date and time and at "TRSDOS II Ready" type **MOUNT {disk name):4** and hit ENTER. If the message "Mounted {disk name} on drive :4 -FP# {ARCNET # of FP)" is displayed, then the Application Processor has successfully mounted the File Processor hard disk.

VI) **Create the system map.** This is one of the most important steps in the **ARCNET™** installation. The System Map will be extremely helpful in any future troubleshooting endeavor. First let us state a few facts about the **ARCNET™** system:

A) Each **ARCNET™** board must have a different identification number. This number is from 1 to FF hex (Zero is not a valid number).

B) In a **ARCNET™** system of 255 computers there will be cables running in all directions.

C) Each computer will be connected to either Passive or Active Hub except in the case of a two computer system.

Keeping these facts in mind you can see that the **ARCNET™** system has the capabilities of becoming a technical nightmare. The System Map is intended to help sort out the complexities of the system. The System Map should contain the **ARCNET™** identity number, unit serial number, the location where it is installed, and the location and type of equipment installed at the other end of the cable. Each computer on the system should be marked on the inside as well as on the outside with its individual **ARCNET™** number. Every Passive and Active Hub should be labeled with a unique identifying number. Each port on the Passive or Active Hub should be listed on the System Map. A copy of the System Map should be maintained and kept up to date by the shop responsible for maintenance of the system. A copy is also to be given to the customer for his files.

ARCNET™ System Example

Figure 2 on page 17 illustrates a fictional ARCNET™ system. In analyzing the system we must remember that:

1) Maximum cable length is 2ØØ feet when using a Passive Hub.

2) A Passive Hub can link up to four units together provided that no cable paths exceed 2ØØ feet.

3) Maximum cable length for an Active Hub is 2ØØØ feet as long there are no Passive Hubs in the cable path.

4) Anytime a Passive Hub is added to a cable path the maximum cable length immediately becomes 2ØØ feet.

5) Two Passive Hubs cannot be connected in series; they would degrade the signal too much.

6) Active Hubs can be connected in series.

7) An Active Hub can be used to make eight cable connections to a maximum cable length of 2ØØØ feet between two Active Hubs or between a computer and a Active Hub.

8) A two computer system can have a maximum cable length of 2ØØØ feet provided there are no Passive Hubs in the cable path.

9) The maximum cable length using Active Hubs 2ØØØ feet apart is 4 miles.

Now we can analyze the system illustrated on page 17.

Passive Hub #3 has 4 units connected to it; three computers and one Active Hub. When analyzing this hub we must look at all cable paths and check to see if any of them exceed 2ØØ feet.

The distance between:

1) Computer "A" and Passive Hub #3.....5Ø feet
2) Computer "B" and Passive Hub #3.....5Ø feet
3) Computer "C" and Passive Hub #3.....5Ø feet
4) Active Hub #2 and Passive Hub #3.....15Ø feet
5) Computer "A" and Active Hub #2.....2ØØ feet
6) Computer "B" and Active Hub #2.....2ØØ feet
7) Computer "C" and Active Hub #2.....2ØØ feet
8) Computer "A" and Computer "B".....1ØØ feet
9) Computer "B" and Computer "C".....1ØØ feet
1Ø) Computer "B" and COMPUTER "C".....1ØØ feet

If any of the above measurements were more than 2ØØ feet then the system would not perform properly, because there is a Passive Hub in the cable path.

ARCNET™ System Example

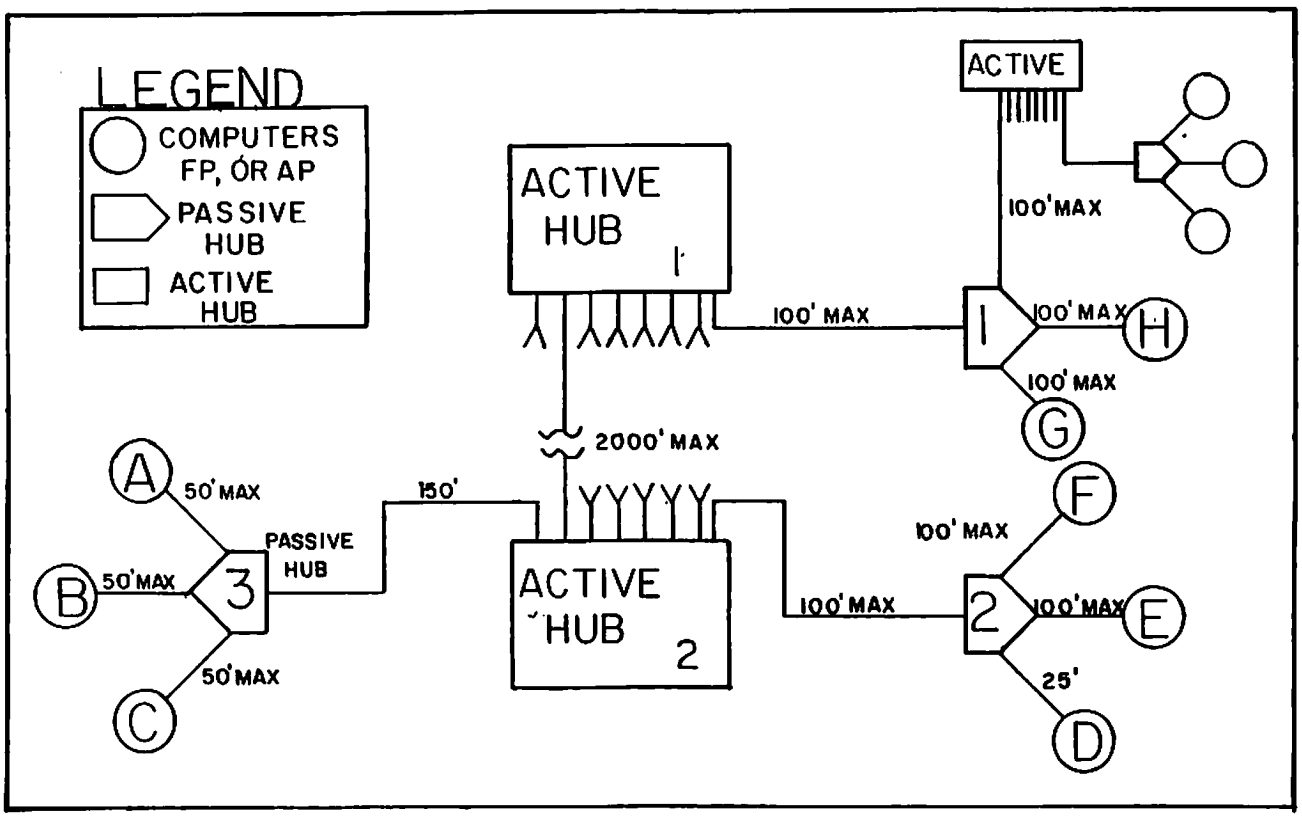


Figure 2

Radio Shack®

ARCNET™ Board Installation

The installation of the **ARCNET™** board is one of the easier steps in the system installation process, but like anything else it can cause its share of problems if it's not done correctly. The following steps will describe the installation process:

1) Thoroughly check the computer the board is to be installed in. If any discrepancies are found then correct them before going any further.

2) If the unit is a Model II:

   A) And DOES NOT have an AXX-6ØØ8 or AXX-6ØØ9 then the power supply must be replaced (see Technical Bulletins II:29, II:37, and II:5).

   B) Power On Reset circuit must be changed (see Technical Bulletin II:25).

   C) Install the Enhanced DMA Mod (see Technical Bulletin II:26).

   D) And if there is no hole for the **ARCNET™** cable connector it must have a new back panel installed (AZ-5223 catalog #26-4ØØ2).

   E) Insure all of the following technical bulletins have been applied.

II:4	Zener diode on old style FDC board
II:5	Modification to Motorola video board
II:9	Old style FDC board modification and alignment
II:1Ø	Trace cut on early design FDC for use with XENIX
II:13	Old style FDC board has C17 backwards
II:16	BOOT ERROR DC on Shugart drive (LSI board only)
II:2Ø	BOOT ERROR's on Shugart drive (Discreet board only)
II:21	Wire jumper on old style FDC boards for precomp
II:23	System lockup or weird keyboard entries
II:28	Cut and jump to correct head load termination
II:31	Missing jumpers on 64K RAM board and HD interface board
II:32	Missing jumpers on CPU board
II:38	Shorting foil for static protection on keyboards

3) If the unit is a Model 16:

   A) The Power On Reset circuit must be changed (see Technical Bulletin II:25).

   B) Insure all of the following technical bulletins have been applied.

16:3	Improve Z8Ø clock on REV D CPU board
16:5	C41 on CPU board is backwards
16:8	Tandon motor speed modification
16:1Ø	Incorrect power supply fuse
16:15	Proper 5 volt supply for AA11Ø82 PSU (AXX-6ØØ9)

4) If the unit is a Model 12, the card cage will have to be installed. If the unit in a Model 16B or 16B+ insure that the following technical bulletins have been applied:

12/16B:2 Reset circuit drive capability
12/16B:3 Correct power up problems with U81
12/16B:5 Card cage interrupt error
12/16B:6 DMA select
12/16B:9 Proper main PCB jumpering for 12's and 16B's
12/16B:1Ø Cooling enhancement kit
12/16B:11 Change in SIO control signals
12/16B:12 Video RAM access timing change
12/16B:13 Change in type of tuning capacitor used in VCO circuit
12/16B:14 Add pull up to PSEL line for printer interface
12/16B:17 Card cage change

5) Install the ARCNET™ connector in the hole using a plastic washer from the outside. Place the other plastic washer on the inside and then screw the nut on and tighten it down snugly. Make sure the connector does not short to the back panel.

6) Install the cable supplied with the ARCNET™ board with the "L shaped" BNC connector towards the bottom. Twist it until it snaps on the connector.

7) **SPECIAL NOTE: ALL ARCNET™ boards MUST be checked to insure compliance with the latest revisions of the ARCNET™ technical bulletins. Pay particular attention to the fact that the transistors (Q1, Q2, and Q3) MUST BE REPLACED and not just turned around. If the transistors were in backwards the RIM8Ø (COM 9Ø26) chip MUST BE REPLACED regardless of the date code, because the chip HAS been damaged even though it may appear to pass the checkout tests.**

ARCNET™:ØØ1 BNC connector installation instructions. 3/1/83
ARCNET™:ØØ2 Proper installation of Q1,Q2, and Q3. 4/12/84
ARCNET™:ØØ3 Some COM9Ø26 LSI chips cause continuous RECONs. 4/13/84
ARCNET™:ØØ4 Proper jumpers for ARCNET™ board. 8/26/83
ARCNET™:ØØ5 Using software as a troubleshooting tool. 11/18/83
ARCNET™:ØØ6 Possible faulty DIP switches. 1/18/84

8) Set the ARCNET™ ID number for the board using dip switch Z26. **Remember that each board must have a unique number from 1 to 255 and Ø is not a valid number.**

9) If the unit is a Model II or a Model 16 install the ARCNET™ board in the third card slot from the right (as viewed from the back of the unit). If the unit has a hard disk installed then install the card in the fourth card slot. Connect the short coaxial cable end to the connector on the board and twist until it snaps in place.

1Ø) If the unit is a Model 12, 16B, or 16B+ install the ARCNET™ board in the first card slot from the bottom. If the unit has a hard disk interface installed then install the ARCNET™ board in the second card slot. Connect the short coaxial end to the connector on the board and twist until it snaps in place.

11) For a Model II, install the 16K RAM board in any open slot if there is no hard disk interface board or Model 16 Enhancement present.

12) If the AXX-6ØØ8 was installed then power up the unit and immediately check the power supply voltages as outlined in Technical Bulletin II:29.

13) Thoroughly test the unit using the system test and cables, and then re-assemble it. Connect the unit to the system and test the ARCNET™ board with at least two known good units using ARCTST.

ARCNET™ System Map

The system maps on the following pages are examples only. There are blanks of each map so copies can be made for your benefit. A description follows:

Cable length: Total cable length from the port to the unit listed in "End of Cable Location".

Cable ID number: Number used to identify the cable ends for example the cable connected to port #5 of Active Hub #5 would be labeled A5-5.

ARCNET™ board number: Individual hex number of the ARCNET™ board. For the hubs map it is the number of the board at the end of the cable. For the computers map this is the number of the board inside.

End of cable location: This is the location of the end of cable and what type of unit is attached to it.

Unit Location: Is the computer's location assigned to the ARCNET™ number and type of unit there. This is used on the computer maps only.

All other categories are self explanatory.

ARCNET™ System Map
Active Hubs

Customer Name: Technical Support

Address: 400 Atrium One Tandy CENTER

Active Hub # 1 SN 800016 Location Ken Brookner's Office

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1	10 '	A1-1	#01	Application Processor Ken Brookner's Office
Port #2	20 '	A1-2	#03	Application Processor Gary Kueck's Office
Port #3	50 '	A1-3	N/A	Active Hub #2 Kellie's File Cabinet
Port #4	5 '	A1-4	#02	File Processor Ken Brookner's Office
Port #5	20 '	A1-5	#05	Application Processor Don Gerber's Office
Port #6	50 '	A1-6	#04	Application Processor Jim Gilbert's Office
Port #7		A1-7		Unused
Port #8		A1-8		Unused

Active Hub # 2 SN 800017 Location Kellie's File Cabinet

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1	50 '	A2-1	N/A	Active Hub #1 Ken Brookner's Office
Port #2	50 '	A2-2	#07	Application Processor Rick Luttrall's Office
Port #3	50 '	A2-3	#08	Application Processor Dave Williams' Office
Port #4	50 '	A2-4	#06	Application Processor Gary Bannister's Office
Port #5	150 '	A2-5	N/A	Passive Hub #1 QC Area
Port #6		A2-6		Unused
Port #7		A2-7		Unused
Port #8		A2-8		Unused

ARCNET™ System Map
Passive Hubs

Customer Name: Technical Support

Address: 4ØØ Atrium One Tandy Center

Passive Hub # 1 Location QC Area

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1	5Ø'	P1-1	# Ø9	Application Processor QC Area
Port #2	5Ø'	P1-2	# ØA	Application Processor QC Area
Port #3	5Ø'	P1-3	# ØB	Application Processor QC area
Port #4	15Ø'	P1-4	N/A	Active Hub #1 Port #5 Kellie's File Cabinet

Passive Hub # ___ Location _____

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				

Passive Hub # ___ Location _____

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				

ARCNET™ System Map
Computers

Customer Name: Technical Support

Address: 400 Atrium One Tandy CENTER

ARCNET# (Hex)	Serial #	Unit Location	End of Cable Location
#01	4506337	Application Processor Ken Brookner's Office	Active Hub #1 Ken Brookner's Off. 10'
#02	4037805	File Processor Ken Brookner's Off.	Active Hub #1 Ken Brookner's Off. 5'
#03	2007553	Application Processor Gary Kueck's Off.	Active Hub #1 Ken Brookner's Off. 20'
#04	2007993	Application Processor Jim Gilbert's Off.	Active Hub #1 Ken Brookner's Off. 50'
#05	2007889	Application Processor Don Gerber's Off.	Active Hub #1 Ken Brookner's Off. 20'
#06	4059489	Application Processor Gary Bannister's Off.	Active Hub #2 Kellie's Off. 50'
#07	206996	Application Processor Rick Luttrall's Off.	Active Hub #2 Kellie's Off. 50'
#08	2008372	Application Processor Dave Williams' Office	Active Hub #2 Kellie's Off. 50'
#09	4056656	Application Processor QC Area	Passive Hub #1 Port #1 QC Area
#0A	4062231	Application Processor QC Area	Passive Hub #1 Port #2 QC Area
#0B	4085541	Application Processor QC Area	Passive Hub #1 Port #3 QC area

ARCNET™ System Map
Active Hubs

Customer Name: _____

Address: _____

Active Hub # ___ SN _____ Location _____

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				
Port #5				
Port #6				
Port #7				
Port #8				

Active Hub # ___ SN _____ Location _____

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				
Port #5				
Port #6				
Port #7				
Port #8				

ARCNET™ System Map
Passive Hubs

Customer Name: ______________________________

Address: ______________________________

Passive Hub # ___ Location ______________________________

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				

Passive Hub # ___ Location ______________________________

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				

Passive Hub # ___ Location ______________________________

Port Number	Cable Length	Cable ID Number	ARCNET Board Number	End of cable Location
Port #1				
Port #2				
Port #3				
Port #4				

Page _____ of _____

ARCNET™ System Map
Computers

Customer Name: _____

Address: _____

ARCNET# (Hex)	CPU Serial #	Unit Location	End of Cable Location

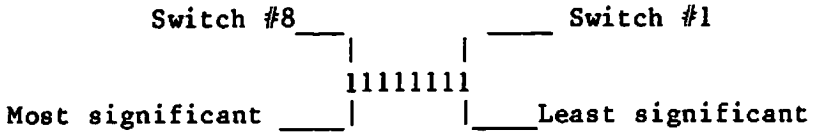
Page _____ of _____

Radio Shack®

APPENDIX A

Switch Conversion Chart

Decimal	Hex	Switch	Decimal	Hex	Switch
1	1	00000001	26	1A	00011010
2	2	00000010	27	1B	00011011
3	3	00000011	28	1C	00011100
4	4	00000100	29	1D	00011101
5	5	00000101	30	1E	00011110
6	6	00000110	31	1F	00011111
7	7	00000111	32	20	00100000
8	8	00001000	33	21	00100001
9	9	00001001	34	22	00100010
10	A	00001010	35	23	00100011
11	B	00001011	36	24	00100100
12	C	00001100	37	25	00100101
13	D	00001101	38	26	00100110
14	E	00001110	39	27	00100111
15	F	00001111	40	28	00101000
16	10	00010000	41	29	00101001
17	11	00010001	42	2A	00101010
18	12	00010010	43	2B	00101011
19	13	00010011	44	2C	00101100
20	14	00010100	45	2D	00101101
21	15	00010101	46	2E	00101110
22	16	00010110	47	2F	00101111
23	17	00010111	48	30	00110000
24	18	00011000	49	31	00110001
25	19	00011001	50	32	00110010



Switch Conversion Chart

Decimal	Hex	Switch	Decimal	Hex	Switch
51	33	00110011	101	65	01100101
52	34	00110100	102	66	01100110
53	35	00110101	103	67	01100111
54	36	00110110	104	68	01101000
55	37	00110111	105	69	01101001
56	38	00111000	106	6A	01101010
57	39	00111001	107	6B	01101011
58	3A	00111010	108	6C	01101100
59	3B	00111011	109	6D	01101101
60	3C	00111100	110	6E	01101110
61	3D	00111101	111	6F	01101111
62	3E	00111110	112	70	01110000
63	3F	00111111	113	71	01110001
64	40	01000000	114	72	01110010
65	41	01000001	115	73	01110011
66	42	01000010	116	74	01110100
67	43	01000011	117	75	01110101
68	44	01000100	118	76	01110110
69	45	01000101	119	77	01110111
70	46	01000110	120	78	01111000
71	47	01000111	121	79	01111001
72	48	01001000	122	7A	01111010
73	49	01001001	123	7B	01111011
74	4A	01001010	124	7C	01111100
75	4B	01001011	125	7D	01111101
76	4C	01001100	126	7E	01111110
77	4D	01001101	127	7F	01111111
78	4E	01001110	128	80	10000000
79	4F	01001111	129	81	10000001
80	50	01010000	130	82	10000010
81	51	01010001	131	83	10000011
82	52	01010010	132	84	10000100
83	53	01010011	133	85	10000101
84	54	01010100	134	86	10000110
85	55	01010101	135	87	10000111
86	56	01010110	136	88	10001000
87	57	01010111	137	89	10001001
88	58	01011000	138	8A	10001010
89	59	01011001	139	8B	10001011
90	5A	01011010	140	8C	10001100
91	5B	01011011	141	8D	10001101
92	5C	01011100	142	8E	10001110
93	5D	01011101	143	8F	10001111
94	5E	01011110	144	90	10010000
95	5F	01011111	145	91	10010001
96	60	01100000	146	92	10010010
97	61	01100001	147	93	10010011
98	62	01100010	148	94	10010100
99	63	01100011	149	95	10010101
100	64	01100100	150	96	10010110

Switch Conversion Chart

Decimal	Hex	Switch	Decimal	Hex	Switch
151	97	10010111	204	CC	11001100
152	98	10011000	205	CD	11001101
153	99	10011001	206	CE	11001110
154	9A	10011010	207	CF	11001111
155	9B	10011011	208	D0	11010000
156	9C	10011100	209	D1	11010001
157	9D	10011101	210	D2	11010010
158	9E	10011110	211	D3	11010011
159	9F	10011111	212	D4	11010100
160	A0	10100000	213	D5	11010101
161	A1	10100001	214	D6	11010110
162	A2	10100010	215	D7	11010111
163	A3	10100011	216	D8	11011000
164	A4	10100100	217	D9	11011001
165	A5	10100101	218	DA	11011010
166	A6	10100110	219	DB	11011011
167	A7	10100111	220	DC	11011100
168	A8	10101000	221	DD	11011101
169	A9	10101001	222	DE	11011110
170	AA	10101010	223	DF	11011111
171	AB	10101011	224	E0	11100000
172	AC	10101100	225	E1	11100001
173	AD	10101101	226	E2	11100010
174	AE	10101110	227	E3	11100011
175	AF	10101111	228	E4	11100100
176	B0	10110000	229	E5	11100101
177	B1	10110001	230	E6	11100110
178	B2	10110010	231	E7	11100111
179	B3	10110011	232	E8	11101000
180	B4	10110100	233	E9	11101001
181	B5	10110101	234	EA	11101010
182	B6	10110110	235	EB	11101011
183	B7	10110111	236	EC	11101100
184	B8	10111000	237	ED	11101101
185	B9	10111001	238	EE	11101110
186	BA	10111010	239	EF	11101111
187	BB	10111011	240	F0	11110000
188	BC	10111100	241	F1	11110001
189	BD	10111101	242	F2	11110010
190	BE	10111110	243	F3	11110011
191	BF	10111111	244	F4	11110100
192	C0	11000000	245	F5	11110101
193	C1	11000001	246	F6	11110110
194	C2	11000010	247	F7	11110111
195	C3	11000011	248	F8	11111000
196	C4	11000100	249	F9	11111001
197	C5	11000101	250	FA	11111010
198	C6	11000110	251	FB	11111011
199	C7	11000111	252	FC	11111100
200	C8	11001000	253	FD	11111101
201	C9	11001001	254	FE	11111110
202	CA	11001010	255	FF	11111111
203	CB	11001011	256	100	100000000

APPENDIX B

RIM8Ø THEORY OF OPERATION

This discussion will concern seven functional areas of the RIM8Ø ARCNET™ interface circuit board. They are listed below:

- Memory section
- Decoding Logic
- Bus Steering Logic
- Interrupt Control Logic
- Integrated RIM Circuit (IRC) and Support Logic
- TRS8Ø/RIM8Ø Control Logic
- ARCNET™ Interface Circuitry

Memory Section

The RIM8Ø board has 1K of RAM (4118) that is indirectly accessible by the Z-8Ø. The 8 input nand gate (Z33) is used to decode addresses in the range of BØ-B7. The bcd to decimal decoder (Z15) decodes the individual addresses. Pin 6 (B5), is used to access the memory location specified by counters Z47 and Z49. Each memory access will cause the counters to increment, pointing to the next memory location. The counters can be set by a write to port B2. The current setting of the counters can be read by an in from port B2, which enables buffer Z37 to gate the data onto the Z-8Ø data bus. The output of the counters does not actually connect to the RAM. The RIM IC reads the address from the counters through Z43 and then supplies the address to the RAM Z24 through a latch (Z44). This works for 256 byte blocks of memory. To access the next block, the Z-8Ø directly sets the bits A8 and A9 at the RAM through DØ and D1 of port B4. A quad 2 line to 1 multiplexer (Z48) is used to select between A8 and A9 of the Z8Ø or RB9 or RB1Ø of the RIM bus.

Decoding Logic

o I/O

The same 8 input nand gate (Z33), decodes the lower eight address bits port selection. The output of Z33 is supplied with AØ-A2 to Z15, a 1 of 1Ø decoder. The output of Z15 is NORed (Z1) with WR* and IOCYC* to produce the clock input to flip-flops Z17 and Z5 for memory selection. Z15 also decodes two I/O addresses for the RIM circuit (Z41) and the four I/O addresses for the Z8Ø CTC (Z34).

o Options and Addresses

The addresses of a normal RIM8Ø board (jumpers E2-E3 & E4-E5) are as follows (In hex):

PORT	FUNCTION
BØ-B1	CTC enables
B2	RAM address register
B3	unused
B4	RAM address bits 8 and 9
B5	Memory
B6-B7	Integrated RIM chip

Optionally, the board can be jumpered for addresses B8-BF, AØ-A7, and A8-AF.

NOTE: Whenever ports BØ-B2 are accessed, the clock to the CTC is disabled by Z2, Z14, and Q1.

Bus Steering Logic

There are three bus steering functions on the RIM8Ø board, one involves the direction of the TRS-8Ø data bus, the second is the direction of the TRS-8Ø data to/from the integrated RIM circuit (IRC) bus, and the third concerns the RIM8Ø buffer memory access.

o TRS-8Ø data bus direction

Octal buffer chip (Z35), is used to buffer data from the RIM8Ø to the TRS-8Ø data bus. It was selected for its high current drive capability (48ma). It is enabled by two thirds of Z1 and one-half of Z13 on; 1) a read cycle (R/W*), 2) an interrupt acknowledge to the CTC, or 3) a read operation from the CTC.

One-half of Z36 an one-half of Z38 are used to buffer data from the TRS-8Ø to the RIM8Ø board. These eight buffers are enabled by one-half of Z32 and an inverter of Z28 on; 1) TRS-8Ø write cycles (WR*), 2) an instruction fetch cycle (SYNC* and RD*). The second case permits the CTC to receive a RETI instruction.

o TRS-8Ø to/from RIM bus

Z43 is a multiplexer that allows the RIM8Ø bus to read the counters (Z47 & Z49) or the Z8Ø data bus, depending on DASEL. The buffer from the RIM8Ø bus to the Z8Ø is Z42, which is enabled by ADIE* from the control logic, and the RWAIT* signal from the IRC.

o RIM8Ø Buffer memory addressing

The memory chip (Z24), has 8 data lines and 1Ø address lines. The lower eight address lines are latched by Z44 by the L- signal from the IRC. The tow most significant address lines from the IRC and the TRS-8Ø (A9 abd A8) are multiplexed by Z48 to permit the correct pair to be presented to the memory. Selection is controlled by the AIE- signal from the IRC.

Interrupt Control Logic

The Z8ØA-CTC (Z34), performs interrupt control for the RIM8Ø. Its peripheral circuitry includes:

1) A TRS-8Ø interrupt line driver, Z6 and Z14.

2) An Interrupt Enable In (IEI) look ahead section, Z2 and Z7, to speed the propagation of the interrupt daisy chain signal.

3) An edge generator (Z28 and Z32) that is enabled by the IRC interrupt signal (INTR), and is used to ensure that the CTC does not miss any interrupts.

4) A clock driver (Q1, C32, R13, R16, R19, and a 74SØ4 inverter Z7) to provide the required 5 volts peak to peak amplitude and fast rise and fall times to the CTC.

Integrated RIM Circuit (IRC) and Support Logic

The IRC is a custom integrated circuit chip that embodies the intelligence of the RIM8Ø. It responds to commands from the TRS-8Ø, handles data transfers between the TRS-8Ø and the RIM8Ø, and manages the protocol and transmission and reception of messages on the ARCNET™. There are three types of support circuitry described below: input damping, ID number serializer, and clock drivers.

o Input Damping

In order to dampen undershoot on TTL input lines to the IRC, 47ohm DIP's (Z4Ø and Z46) are used in series with those input lines.

o ID Number Serializer

The ID number is selected by switches on Z26 with pull ups on Z25. The 74LS166 (Z3Ø) will, in response to the IDLD- signal of the IRC, serialize the ID number on to IRC input line IDDAT.

o Clock Drivers

IRC clock signal (CLK) is a 5Mhz clock produced by the 2ØMhz crystal (Z29), flip-flop pair Z4, and a 5 volt peak to peak driver (Q3, C21, C31, R18, R15, and a 74SØ4 inverter Z2Ø). It is used for timing of the RIM bus arbitration, and RECON time out. The output of the flip-flop pair in called TTLCLK and is used to clock the ID serializer. The other clock (CA) is also a 5Mhz clock and is turned on and off by DSYNC- and RX. It and 5 volt peak to peak driver (Q2, C2Ø, C3Ø, R17, R11, R14, and a 74SØ4 inverter Z2Ø). The CA clock is used to drive the ROM sequencer in the IRC.

Interrupt Control Logic

The Z80A-CTC (Z34), performs interrupt control for the RIM8Ø. Its peripheral circuitry includes:

TRS-8Ø/RIM8Ø Control Logic

This circuitry provides interface signals that are required by the TRS-8Ø, the IRC, and other RIM8Ø logic. Its inputs are gathered from these same elements. There are seven signals that are produced; each are discussed below.

o Memory Request (MREQ-)

This signal for the IRC is produced from decoder logic memory request and the B5* signal. These are NOR'ed by one-fourth of Z27 to yield MREQ-.

o I/O Request (IOREQ-)

This signal for the IRC is produced from the decoder logic I/O request signal and the TRS-8Ø IOCYC* signal. These are NOR'ed by one-fourth of Z27 to yield IOREQ-.

o Address Strobe (AS)

The AS signal is used to indicate to the IRC that there is a memory or I/O operation pending. The two NOR outputs above (MEMQ and IOREQ) are NOR'ed together to yield an active low "RIM8Ø addressed" signal or RIMADD- (Z31 pin 3). The upward going edge of AS is produced by the NOR gate (Z6) when RIMADD- goes to zero. The trailing edge is formed when MREQ or IOREQ is clocked through the flip-flop Z5. This high from the Q output will drive the Z6's output low. Different phases of the TRS-8Ø clock must be used (Z7 inverter) to drive the clock inputs of flip-flop Z5 in order to achieve proper AS timing. This is because MEMCYC* and IOCYC* have different relative timing to the TRS-8Ø clock.

o Read/Write (R/W)

This signal indicates to the IRC whether a read or write operation is being performed by the TRS-8Ø. It is produced by the TRS-8Ø RD* signal NOR'ed (Z32) with the RIMADD- signal. R/W also is used by the bus steering logic.

o Data Enable (DATEN-)

The R/W signal is inverted (Z7) to yield DATEN-, which is also used by the bus steering logic.

o WAIT*

This is the TRS-8Ø wait signal. Since the IRC wait signal becomes active too late to permit proper data transfer operations, RIMADD- is used to set a latch (one-half of Z16) that drives WAIT* active (low). However, the trailing edge of the IRC wait is used to reset the latch and to disable the open collector NOR driver (Z6) thereby returning WAIT* to its inactive (high) state.

o Data Select (DATSEL)

DATSEL is produced by a latch (one-half of Z2) that is set by IRC signal ILE- and reset by the IRC signal wait. It is used by the bus steering logic.

ARCNET™ Interface Circuitry

There are three sections of ARCNET™ interface circuitry: 1) the Coax coupler, 2) the transmitter, and 3) the receiver.

o Coax Coupler

This section serves as the link between the transmitter and the receiver sections. Its primary component is transformer T1 that isolates the RIM8Ø from the network. Components C29, R3 and R4 act as a low pass filter to prevent undesirable and unwanted RF emissions from the ARCNET™ coaxial cable. C25 and
C19 are for decoupling, and C28 and R22 provide the required line termination impedance.

o Transmitter

Flip-flops Z23 and Z22 provide one pulse to each line driver, Z12 and Z11 during the period of clock CA whenever TX- from the IRC is active. The pulse to Z11 will occur during the first half of CA to produce a positive voltage across T1 and the pulse to Z12 will occur during the second half of CA to produce a negative voltage across T1. Thus, the on/off keyed bipolar pulses of ARCNET™ are created. Components R2Ø, R21, L4, and L5 dampen pulse rise times to reduce the high frequency components of the ARCNET™ signal.

o Receiver

The receiver section converts the bipolar pulses to TTL pulses. Components R1, R2, L1-L3, C17, C18, C26, C27, and R5-R9 restructure the pulses to compensate for line losses. Differential line receiver (Z1Ø) converts the pulses to TTL levels which are then converted into a pulse train synchronized with the clock of the IRC by Z9, half of Z8, Z19, Z3, and Z17.

APPENDIX C

Active Hub Theory of Operation

The Active Hub is transponder-type device which will allow an uninterrupted distance between two directly connected active elements (Computers or Active Hubs) of up to 2ØØØ feet. The Active Hub's purpose is to receive a signal from one (and only one) channel and transmit a amplified signal out the remaining channels. In a fully loaded system (all eight connectors of the Active Hub in use), one of the connectors will be transmitting data.

Power on Reset

When the power switch is first turned on, C24 starts to charge through R18. At this time, a logical low is applied to inverter U11, pin 1 and its output goes high. The high at pin 2 of U11 is passed to a second inverter at pin 3, and pin 4 outputs a low to reset the system's digital components.

And gate U1Ø, pin 6, goes low, resetting the outputs of latch U8. Also, pin 6 is fed to the inputs of two AND gates, and the outputs at pins 3 and 11 force the D flip-flops (U12 through U16) to preset their Q outputs high. Finally, U1Ø, pin 6 resets the SET-RESET flip-flop made up of parts of U1Ø, U11, and U17.

A few milliseconds later, C24 will force a high at the input of U11, pin 1. The reset cycle is now complete with the following states:

Latch U8's outputs are low; the flip-flops, U12 through U16, have been preset; and the SET-RESET flip-flop has been reset.

At this point, the Active Hub is DC stable, without any AC signal activity at all. This may seem kind of strange - as with all the components in the Active Hub, there is no signal activity after power on. When an input does enter the Hub, all wave shapes generated will be quite narrow (less than 2ØØ nanoseconds).

Analog Signal Processing

Each of the eight channels is set up to transmit or receive. They cannot do both at the same time (the digital logic will not allow that).

The primary side of the pulse transformer is made up of a BNC connector and a resistor network. The resistor network is used to current limit any high voltage transients that may be presented to the Coax cable, and to discharge any accumulated static charges.

The transmit side of any channel is made up of two dual, high current driver packages. One package handles the positive cycle and the other package handles the negative cycle of the output pulse. These drivers will go to a logic low on the outputs to allow current to flow through the pulse transformer. Two inductors and a snubbing network are used to minimize any switching noise generated when the transmitters turn on.

The receiver side of the analog circuitry is made up of a balanced line receiver and a passive wave shaping filter. Its output if normally low, unless; a pulse from the transformer pulls the receiver out of balance. The three resistors at the input of the receiver (two 1ØK's and a "shorting", 1.1K resistor) are used to balance the receiver.

Aside from the coupling capacitors which feed the balancing resistors, the rest of the coils, capacitors, and resistors form a filtering network. This network removes any switching noise picked up by the long coaxial cables connected to the Active Hub. It also pulse shapes the input waveform slightly before the signal is applied to the balanced receiver.

Signal Input Response

Refer to Figure 3, the Timing Diagram.

Depending on which channel first receives an input signal, one of the D flip-flops will be clocked by the rising edge of one of the receiver outputs. If we assume that RX-1, at pin 4 of U3, outputs a rising edge, (waveform A) U12, pin 3, clocks. Since pin 2, the D input, is zero (U8's outputs were reset during the power-up cycle) the Q output at pin 5 goes low (waveform B). Pin 2 of U14 sees the falling edge, and outputs a rising edge to pin 9 of U11 (waveform C). The resulting falling edge at pin 9 of U1Ø (waveform D) causes the set/reset flip-flop to set, and output a rising edge at pin 12 of U11 (waveform E).

This rising edge is used to start two functions. It forces channels 2 through 7 to be transmitters, and it verifies channel 1 as the receiving channel and uses this input to generate the data for the transmitting channels.

The transmitting channels are committed by the rising edge from U11, pin 12 passing through the AND gate made up of U17 and U11. The rising edge at pin 6 of U11 (waveform F) clocks U8. The clocking of U8 set all of its outputs high (waveform N) except for the output pin that is transmitting (waveform G, pin 2).

This is true because all of the D flip-flop's Q outputs are high, except for the transmitting channel. The Q outputs are fed to the inputs of U8. When the clock pin is activated, the input data to the latch is transferred to the outputs and stored. The outputs of U8 are fed to inverters U7 and U9 which enables the transmitter side of all channels (waveform Ø) except for the one that has a logical high fed to it (in this case, channel 1).

U8's outputs are also fed back to the D inputs of the flip-flops, U12 through U16. This feedback loop prevents further clocking of the D flip-flops from having any effect on the cycle just started. Channel 1 is committed as the receiving channel, and other receiver inputs cannot disrupt this cycle.

The data for the transmitting channels is supplied by the rising edge and applied to pin 11 of U17. The output of U17, pin 8, goes low (waveform H) and starts the delay cycle through the digital delay line, DD1.

Twenty-five nanoseconds after the falling edge at pin 1 of DD1, pin 12 goes low (waveform I). This low enables the TX+ sides of all seven channels. Current flow is from the center tap of all transmitting transformers, TXØ1, pin 1, through the inductors LXØ5 and into pins 3 and 5 of UXØ2. The resulting signal is shown in waveform S as the "positive cycle". (The X in the part number can be replaced with the digits 2 through 7. That is, T2Ø1, L4Ø5, U6Ø2, etc.)

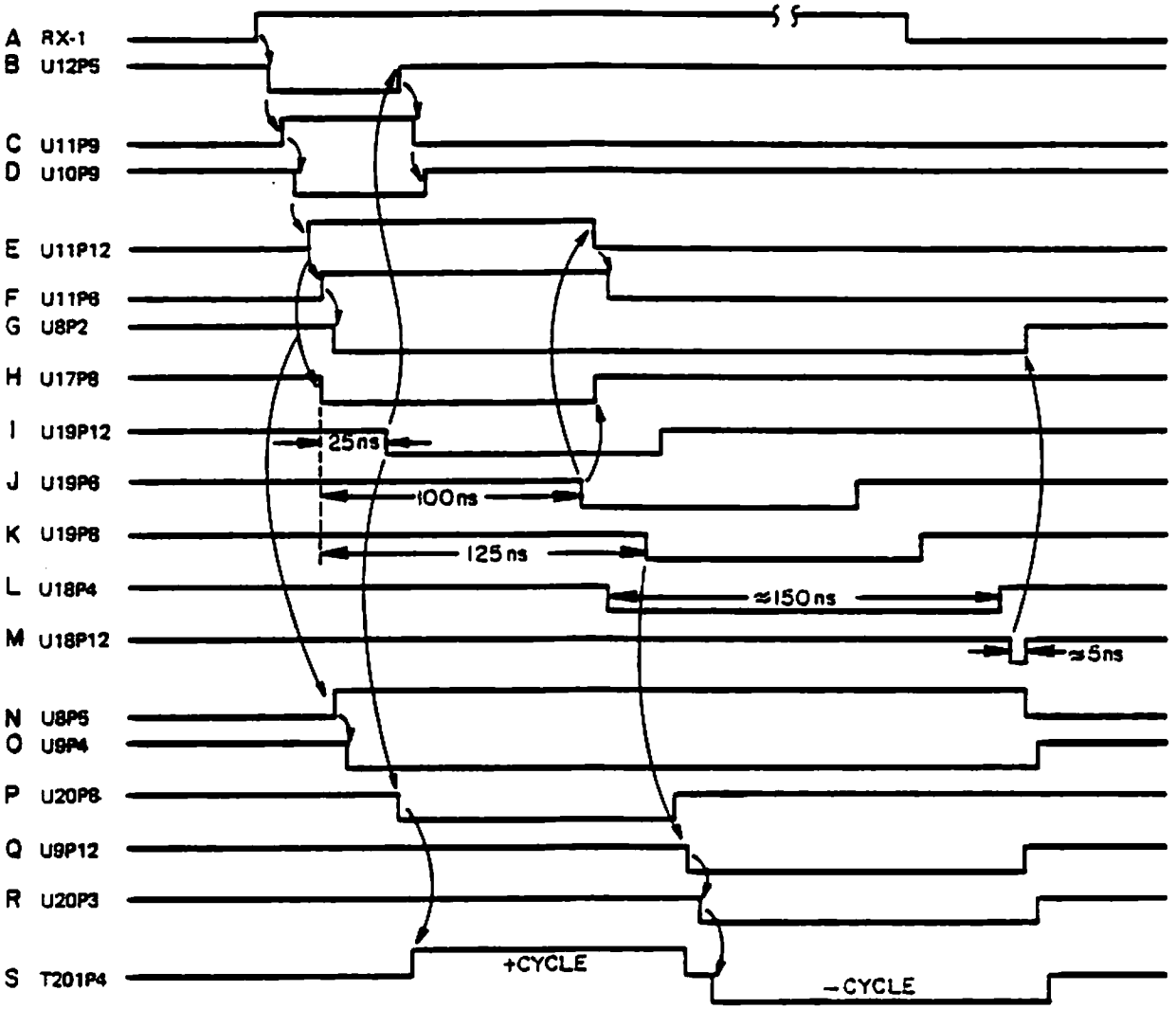
At the same time the TX+ side of all seven channels are activated and the falling edge at pin 12 of DD1 presets all the D flip-flops back to their power-up state. This is accomplished by forcing the preset input pins low on the flip-flops, due to the falling edge at pins 3 and 11 of U1Ø.

Pin 6 of DD1 goes low (waveform J) 1ØØ nanoseconds after the TX+ sides are enabled. This signal is used to force pin 8 of U17 high, thereby ending a low pulse 1ØØ nanoseconds wide, at pin 1 of DD1. The falling edge at pin 6 of DD1 is also used to reset the set/reset flip-flop back to its power on, or inactive state.

When pin 12 of U11 (part of the flip-flop) resets, it starts a delay by triggering U18, pin 1. Pin 4 of U18 goes low and stays low for about 15Ø nanoseconds (waveform L).

While pin 4 is timing out, and 125 nanoseconds after the falling edge at pin 1 of DD1, pin 8 of this delay line goes low (waveform K). The TX- side of all transmitting channels are enabled at this time (the TX+ cycle ends here too). Current flow center tap of TXØ1; out pin 3; through LXØ4 and into pins 3 and 5 of UXØ1. The two inverters in series with pin 8 of DD1 are used to minimize the overlap time between the positive cycle and the negative cycle (waveform S.)

Approximately twenty-five nanoseconds after the end of the TX- cycle (pin 8 of DD1 returns high), U18, pin 4, has timed out, activating U18, pin 12 (waveform M). This pin goes low for only about five nanoseconds which clears latch U8 and presents U12 through U16 a second time in the cycle. All of the logic in the Active Hub is now back to power on, or to an inactive state. The system is now ready to receive another pulse on one of the RX lines, which will start the process all over again.



NOTES:
1. SCALE = 5nsec PER SQUARE
2. ALL GATE DELAYS SET TO 5ns
3. CURVED ARROWS SHOW SEQUENCE

Figure 3 - Timing Diagram for ARCNET™ Active Hub

Hints and Suggestions

1) The pinout on the pulse transformers is backwards from that of IC convention. Pin 6 is indicated at the dot on the package, not pin 1!

2) The pulse width at pin 4 should be longer than the rising edge of the waveform at U19, pin 8. If it is too short, the negative cycle pulse width will be shortened. Since the pulse from pin 12 of U18 is only used to reset the latch, the pulse width should be just long enough to do that. The timing of both pulses added together should not exceed 200 nanoseconds, or "next pulse masking" can occur and data will be lost.

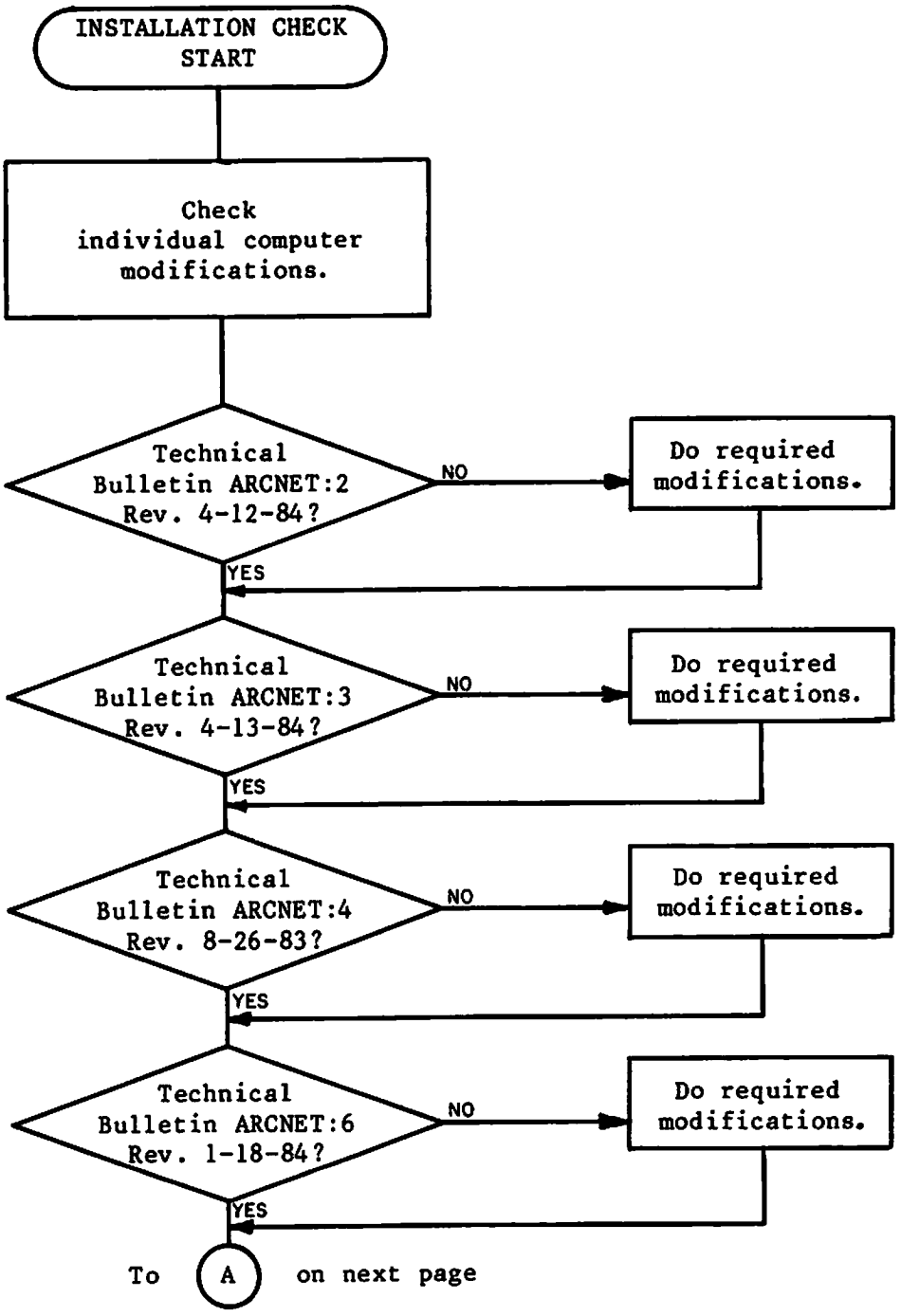
3) The "S" type TTL parts used in the system were put in there for timing reasons. The critical paths where these parts are needed are the D-latches and the logic used with the delay line (DDL).

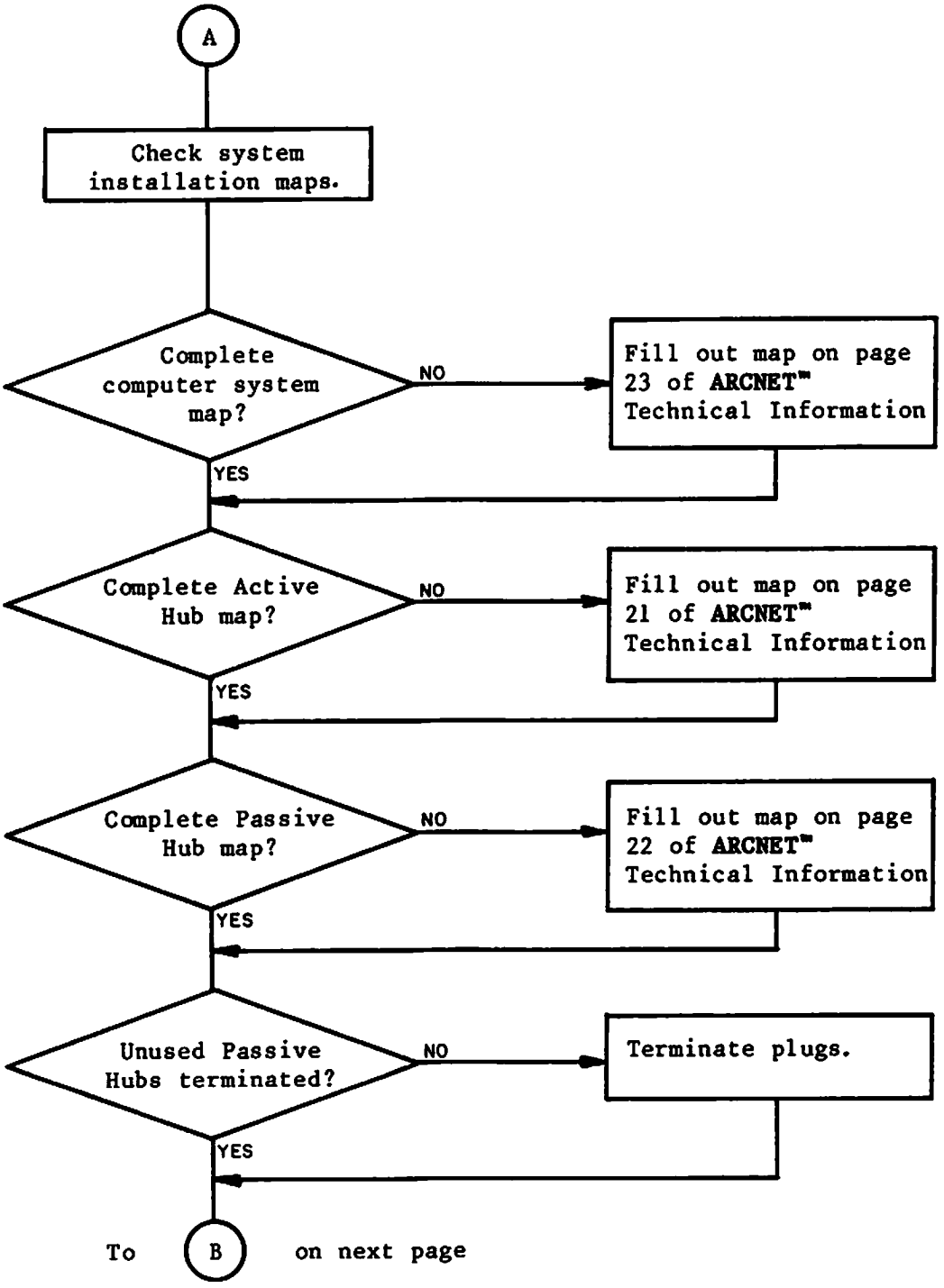
4) The transmitter drivers are high speed devices that drive over a half an amp of current. These parts should only be replaced with devices having the same part number - 75453ATC. A standard 75453 driver is much too slow, and should not be used.

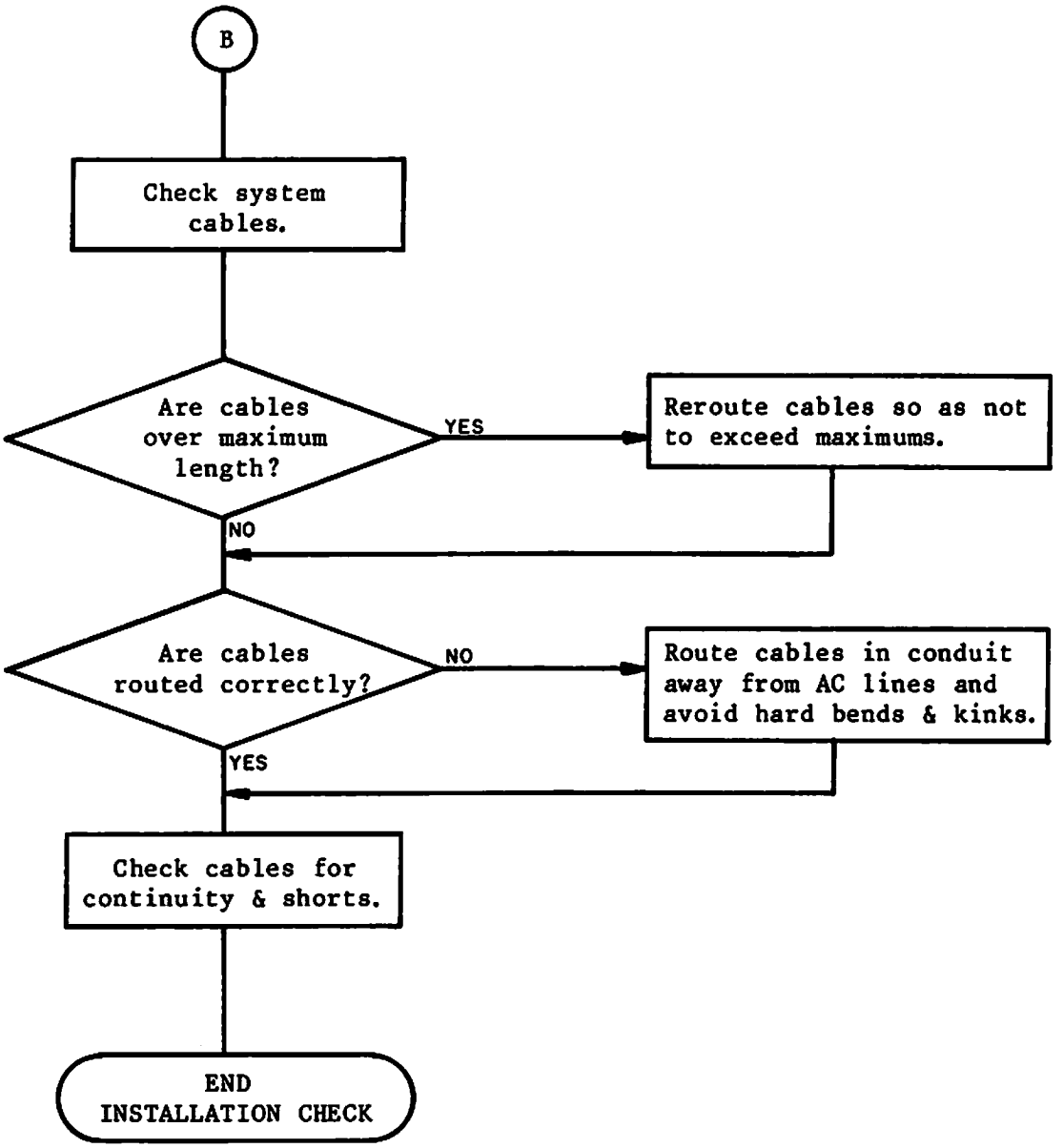
5) Notice that the capacitors used near the BNC connectors are quite large and have a breakdown voltage of at least 1.51K volts. Networks having long coax runs can charge up to large potentials with just static alone. If one of these parts needs replacing, use a capacitor with the proper voltage rating.

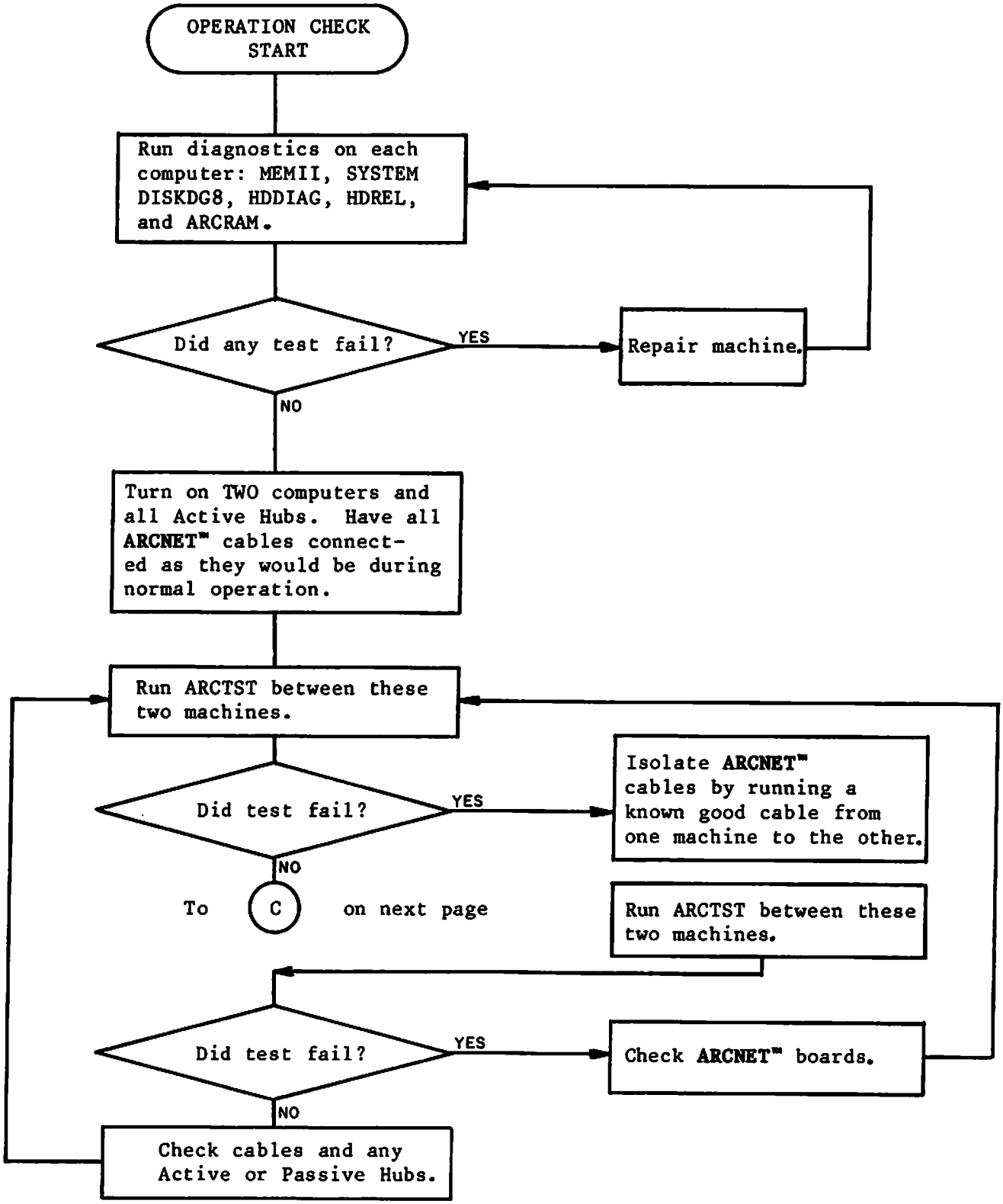
6) Each line receiver package (U3 through U6) supports two channels. Make sure you are looking at the proper pin of these parts when you are troubleshooting a certain channel.

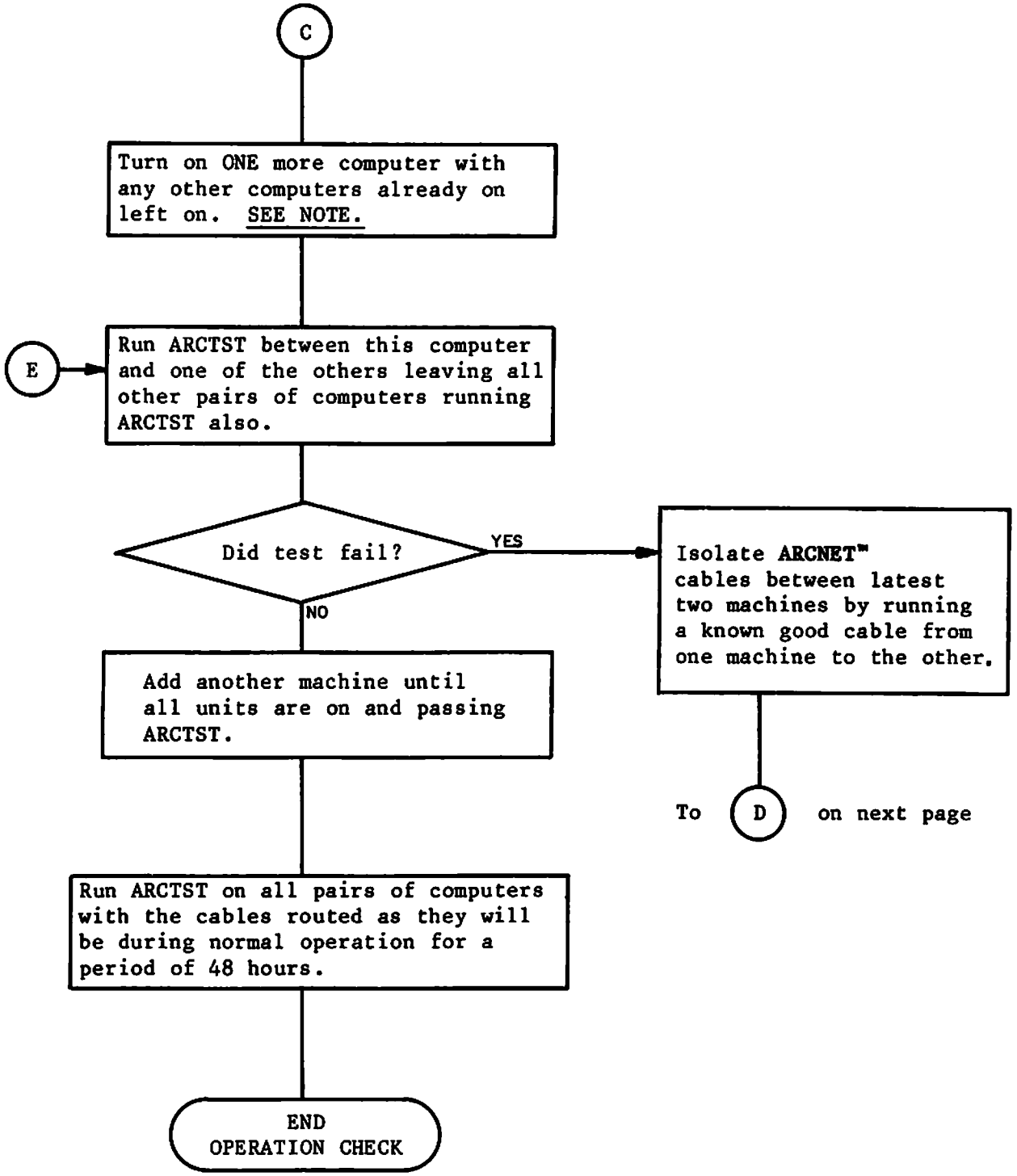
APPENDIX D

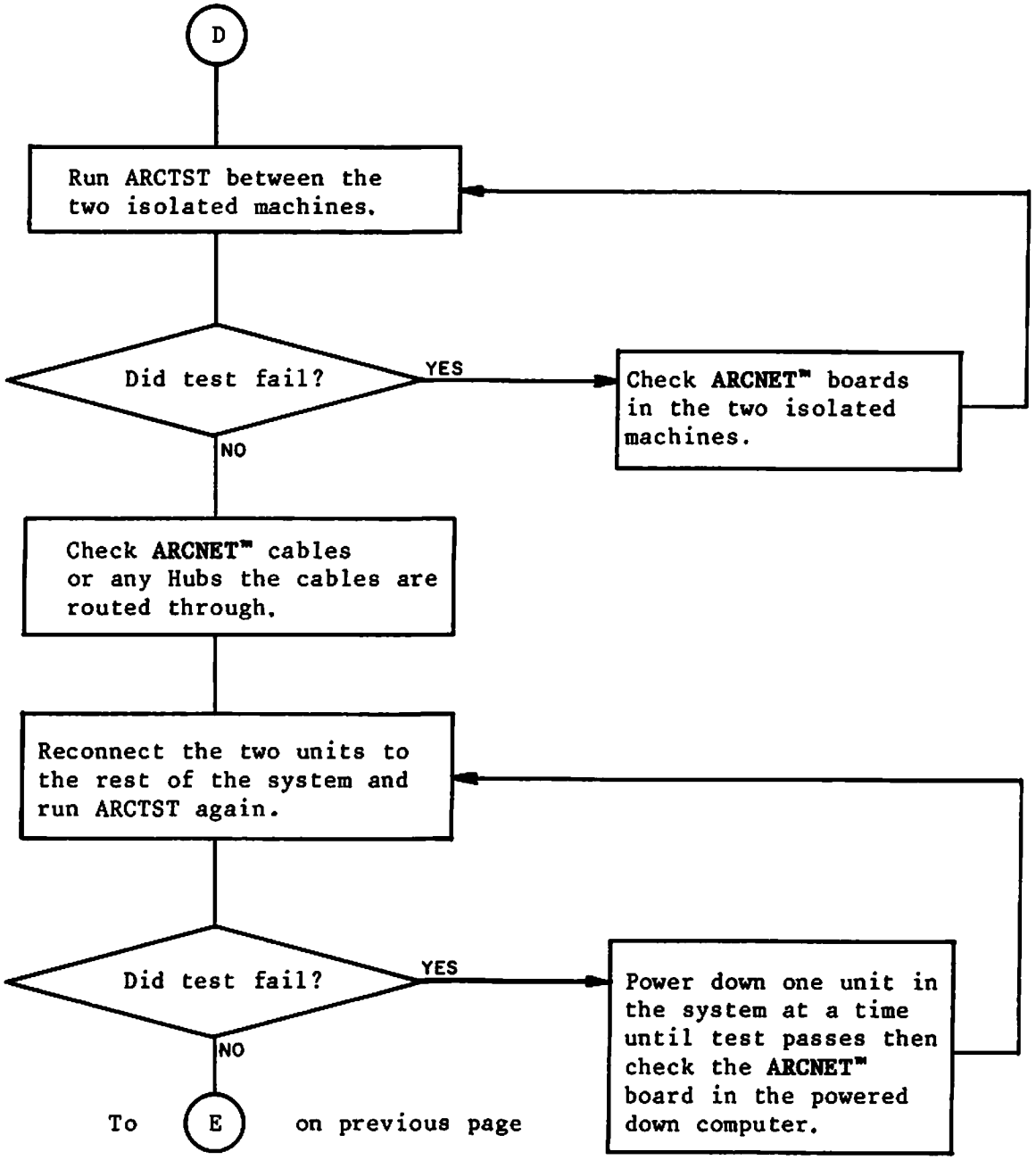












NOTE: Whenever a computer is turned on and connected to the ARCNET™ system, even at INSERT DISKETTE, the ARCNET™ board is active and can cause errors to show up on other units.

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